AN1124

1M to 4M DRAM Upgrading

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INTRODUCTION

Standards set through JEDEC and EIAJ allow upward compatibility from the 1M to 4M DRAM by using the same pinout for SOJ and ZIP packages. Such standards are set to ensure a stable DRAM supply when higher density memories are introduced. This eliminates the need for expensive redesigns of systems that can utilize the new memories.

Although the common pinout between the 1M and 4M DRAM requires little, if any, relayout of the PCB, caution must be exercised when upgrading because of potential incompatibilities with refresh and power up. Both of these involve differences in test mode entry between the 1M and 4M DRAM.

REFRESH

The dynamic memory cell is based on capacitor charge storage for each bit in the array. This charge will dissipate over time, so the entire array must periodically be refreshed to maintain the correct bit state. This is accomplished by cycling through all the rows of the array within a specified refresh time.

The 4M DRAM has 1024 rows instead of the 1M's 512 rows. Since the refresh period of the 4M is twice that of the 1M DRAM, the equivalent wait state of the 4M is the same as that of the 1M. This is summarized in Table 1.

Like the 1M DRAM, the 4M DRAM can be refreshed through a variety of ways: any read or write cycle, a $\overline{RAS}$-only refresh, a $\overline{CAS}$ before $\overline{RAS}$ refresh, or a hidden refresh. A potential incompatibility between the 1M and 4M DRAM exists with the use of the $\overline{CAS}$ before $\overline{RAS}$ refresh.

On the 1M DRAM, the $\overline{W}$ pin is specified as a don't care during the $\overline{CAS}$ before $\overline{RAS}$ refresh. But on the 4M DRAM, the $\overline{W}$ pin must be high (disabled) for time t_{WRP} before $\overline{RAS}$ goes low and held high for time t_{WRH} after the transition. This will prevent the device from entering the JEDEC standard test mode. Figure 1 shows the $\overline{CAS}$ before $\overline{RAS}$ refresh timing for the 4M DRAM, and Figure 2 shows the test mode entry timing. The test mode is exited by performing either a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. Test mode on the 1M DRAM is entered through use of a "supervoltage" on a separate test function pin, and is therefore completely unlike the 4M test mode entry.

POWER UP

Another potential incompatibility between the 1M and 4M DRAM occurs during the power up, and this must be addressed when upgrading. Both devices require a pause of 200 µs after power up, followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed. The pause allows the internal substrate generator to establish the correct bias voltage. The 8 $\overline{RAS}$ cycles initialize all dynamic nodes within the RAM.

To prevent the 4M DRAM from entering the test mode, the 8 $\overline{RAS}$ cycles should be $\overline{RAS}$-only refresh cycles or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. If these refresh modes are not used, the device could power up in the test mode, which can only be exited by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

SUMMARY

Upgrading a system from a 1M DRAM to a 4M DRAM is easily accomplished if a few precautions are taken. The $\overline{CAS}$ before $\overline{RAS}$ refresh mode on the 4M DRAM requires that $\overline{W}$ be high during the $\overline{RAS}$ low transition. If $\overline{W}$ is a don't care, as on the 1M DRAM, the test mode could inadvertently be entered. Caution with the 4M DRAM must also be exercised during the power up. The 8 initialization cycles should be either $\overline{RAS}$-only refresh cycles or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, so that the device comes up in its normal operating mode and not in the test mode.

Table 1. Comparison of Refresh Requirements for the 4M and 1M DRAM
(Times Shown are for Devices with 70 ns Random Access Times)

	4M		1M	
	Normal Power	**Low Power**	**Normal Power**	**Low Power**
Number of Rows	1024	1024	512	512
Number of Bits per Row	4096	4096	2048	2048
Refresh Period (t_{RFSH})	16 ms	128 ms	8 ms	64 ms
Distributed Refresh Period	15.6 µs	124.8 µs	15.6 µs	124.8 µs
Burst Refresh Period	16 ms	128 ms	8 ms	64 ms
Time to Refresh 1 Row (t_{RC})	130 ns	130 ns	130 ns	130 ns
Cumulative Time to Refresh the Entire Array	133.1 µs	133.1 µs	66.6 µs	66.6 µs
Refresh Time/Operating Time	0.833%	0.104%	0.833%	0.104%

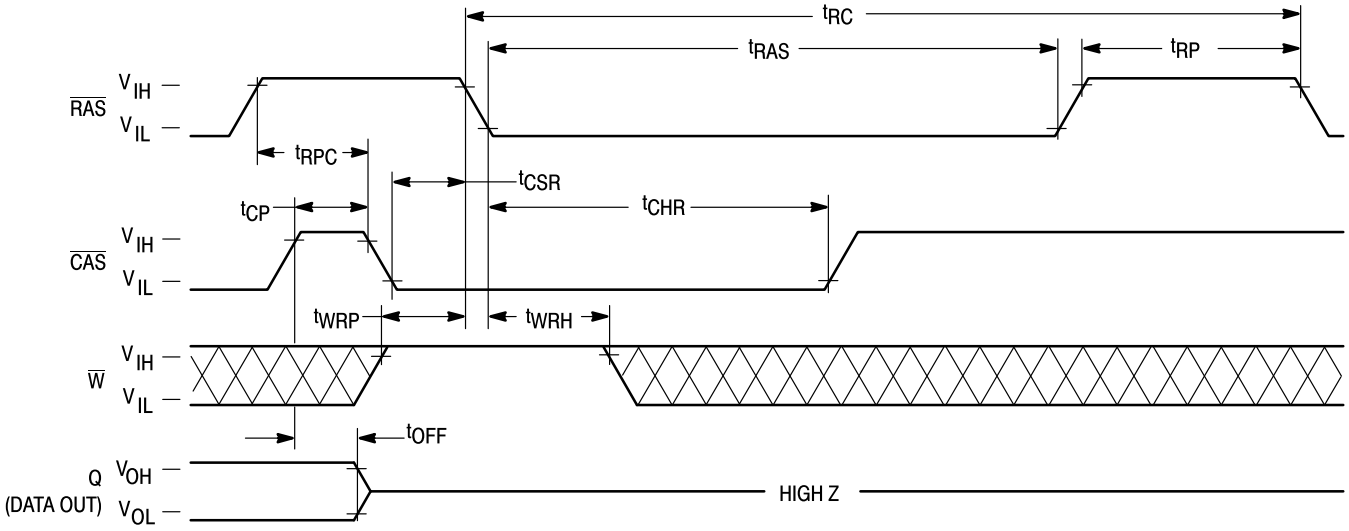

Figure 1. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Timing for the 4M DRAM
(Addresses and $\overline{\text{G}}$ are Don't Care)

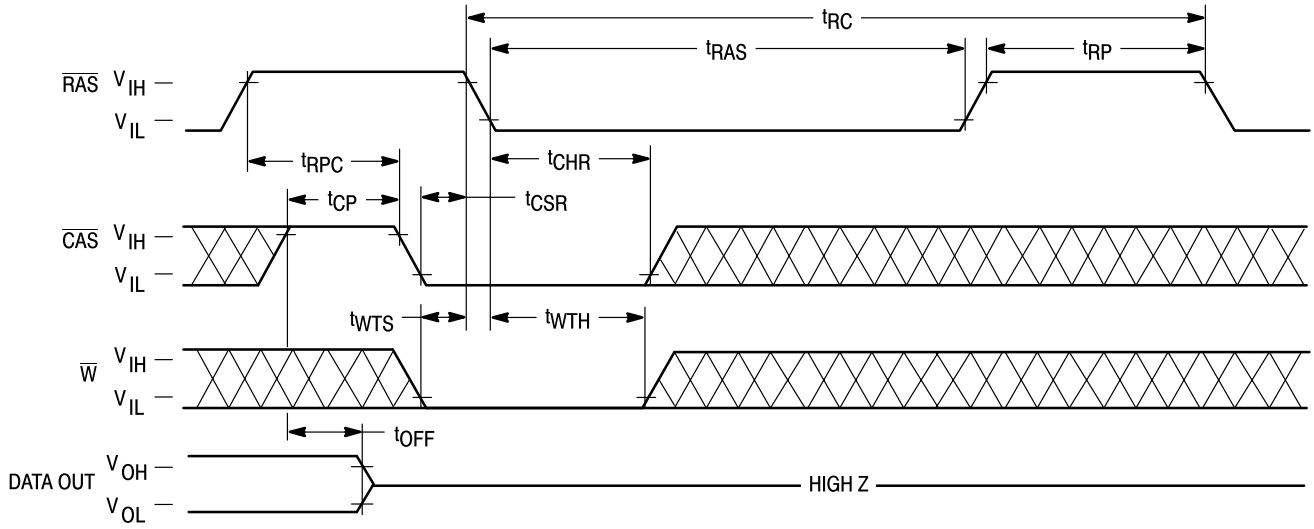

Figure 2. Test Mode Entry Timing for the 4M DRAM

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