



# PC Card (PCMCIA) Interface Switch—12-V Suspend Capability

## FEATURES

- Programmable  $V_{CC}$  Ramp
- Smart Switching
- 12-V Sleepmode Compatible
- Extremely Low  $R_{ON}$
- Reverse Blocking Switches
- $V_{PP}$  Programmable to 0, 12-V or  $V_{CC}$
- Safe Power-Up
- Low Power Consumption
- PC Card 3-V/5-V Compatible
- Logic Compatible Inputs
- Single SO-16 Package

## DESCRIPTION

The Si9712DY combines low on-resistance with slow ramp time and smart switching for overall best performance in integrated PC Card interface switches.

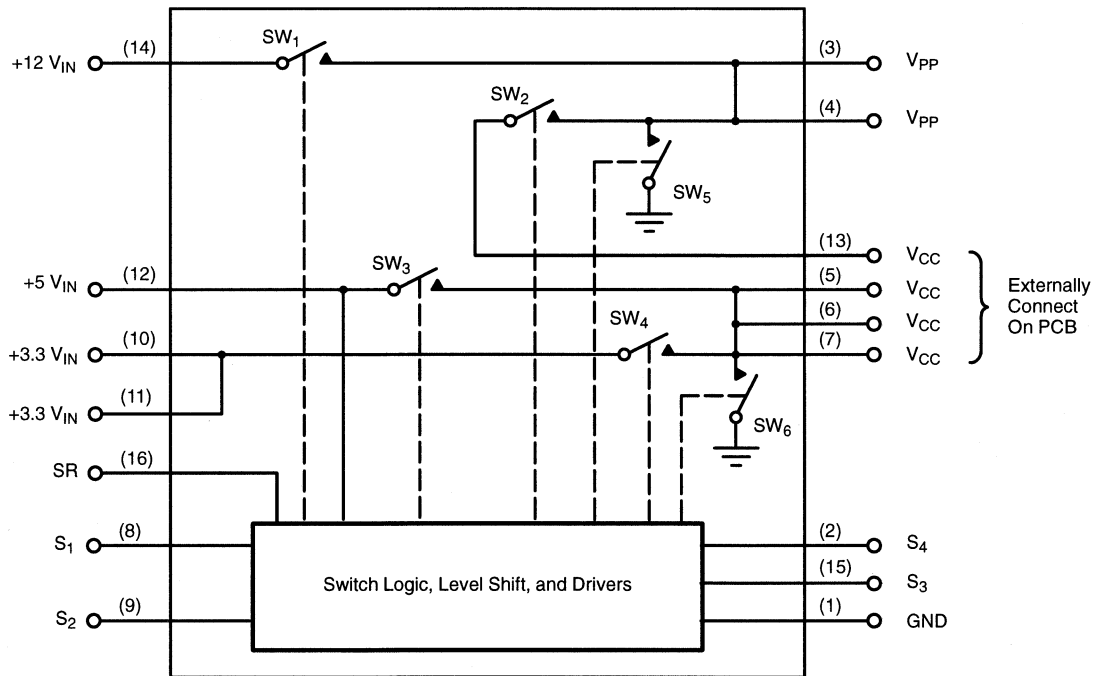
The Si9712DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against an external control input error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9712DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These

control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9712DY complies with the release of the PC Card standard by supplying 0 V, 12 V, and  $V_{CC}$  to the  $V_{PP}$  output and 0 V, 3.3 V, and 5 V to the  $V_{CC}$  output. The  $V_{CC}$  ramp time is user programmable with an external capacitor connected to the SR pin.

The PC Card switch is packaged in a narrow body SO-16 package and is rated over the industrial temperature range -40 to 85°C.

## FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to Ground

+12 V <sub>IN</sub> .....	15 V
+5 V <sub>IN</sub> .....	7 V
+3.3 V <sub>IN</sub> <sup>a</sup> .....	7 V
S <sub>1</sub> through S <sub>4</sub> (CMOS Inputs) .....	7 V
I <sub>OUT</sub> V <sub>PP</sub> <sup>b</sup> .....	300 mA
All Pins .....	-0.5 V
I <sub>OUT</sub> V <sub>CC</sub> <sup>a</sup> .....	4 A

PD Max: (T <sub>A</sub> = 25°C) .....	2.5 W
(T <sub>A</sub> = 85°C) .....	1.0 W
Junction Temperature .....	125°C
Thermal Rating-R <sub>θJA</sub> .....	40°C/W

Notes

- a. Pins 10, 11 connected together externally.  
 b. Pins 3, 4 connected together externally.  
 c. Pins 5, 6, 7, 13 connected together externally.

**RECOMMENDED OPERATING CONDITIONS**

+12 V <sub>IN±</sub> .....	0 or 12 V ± 10%
+5 V <sub>IN</sub> (must be present) .....	5 V ± 10%
+3.3 V <sub>IN</sub> <sup>a</sup> .....	3.3 V ± 10%
C <sub>SR</sub> .....	33 nF
I <sub>OUT</sub> V <sub>PP</sub> <sup>b</sup> .....	150 mA
I <sub>OUT</sub> V <sub>CC</sub> <sup>c</sup> .....	2 A

V <sub>PP</sub> Load Capacitance .....	10 μF Max
V <sub>CC</sub> Load Capacitance .....	150 μF Max

Notes

- a. Pins 10, 11 connected together externally.  
 b. Pins 3, 4 connected together externally.  
 c. Pins 5, 6, 7, 13 connected together externally.

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified C <sub>SR</sub> = 33 nF, +12 V <sub>IN</sub> = 12 V, +5 V <sub>IN</sub> = 5 V +3.3 V <sub>IN</sub> = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits 40 to 85°C			Unit
				Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Switch 1</b>							
On-Resistance	R <sub>ON</sub>	I = 120 mA, +12 V <sub>IN</sub> = 11.4 V S <sub>3</sub> = S <sub>1</sub> = High, S <sub>2</sub> = S <sub>4</sub> = Low	T <sub>A</sub> = 25°C			120	mΩ
			T <sub>A</sub> = 85°C			145	
Off Current (+12 V <sub>IN</sub> )	I <sub>OFF</sub>	+12 V <sub>IN</sub> = 12.6 V S <sub>1</sub> = Low	T <sub>A</sub> = 25°C			1	μA
			T <sub>A</sub> = 85°C			10	
Switching Time	t <sub>SW1(on)</sub>	S <sub>2</sub> = S <sub>4</sub> = Low, See Figure 1. S <sub>3</sub> = High		50	200	350	μs
	t <sub>SW1(off)</sub>			1.0	100		
Delay Time	t <sub>d(on)</sub>	See Figure 3. S <sub>2</sub> = S <sub>4</sub> = Low		1.0	6	20	ms
	t <sub>d(off)</sub>			0.1	2.9	10	
Rise Time	t <sub>SW1(on)</sub>	S <sub>2</sub> = S <sub>4</sub> = Low, S <sub>3</sub> = High, See Figure 2.		50	150	300	μs
<b>Switch 2</b>							
On-Resistance	R <sub>ON</sub>	I = 120 mA, S <sub>2</sub> = S <sub>3</sub> = High S <sub>1</sub> = S <sub>4</sub> = Low	T <sub>A</sub> = 25°C			150	mΩ
			T <sub>A</sub> = 85°C			180	
Switching Time	t <sub>SW2(on)</sub>	S <sub>1</sub> = S <sub>4</sub> = Low, S <sub>3</sub> = High, See Figure 1.		50	200	350	μs
	t <sub>SW2(off)</sub>			1.0	10		
Delay Time	t <sub>d(on)</sub>	S <sub>1</sub> = S <sub>4</sub> = Low, See Figure 3.		1.0	6	20	ms
	t <sub>d(off)</sub>			0.1	1.7	10	
Rise Time	t <sub>SW2(on)</sub>	S <sub>1</sub> = S <sub>4</sub> = Low, S <sub>3</sub> = High, See Figure 2.		50	150	300	μs



<b>SPECIFICATIONS</b>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $C_{SR} = 33 \text{ nF}$ , $+12 V_{IN} = 12 \text{ V}$ , $+5 V_{IN} = 5 \text{ V}$ $+3.3 V_{IN} = 3.3 \text{ V}$ , Low $\leq 0.8 \text{ V}$ , High $\geq 2.2 \text{ V}$	Limits 40 to 85°C			Unit	
			Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>		
<b>Switch 3</b>							
On-Resistance	$R_{ON}$	$I = 500\text{mA}$ , $S_3 = \text{High}$ $S_1 = S_2 = S_4 = \text{Low}$	$T_A = 25^\circ\text{C}$		70	m $\Omega$	
			$T_A = 85^\circ\text{C}$		95		
Off Current ( $V_{CC}$ )	$I_{OF}$	$+5 V_{IN} = 5.5 \text{ V}$ , $V_{CC} = 0 \text{ V}$ $S_1 = S_2 = S_3 = \text{Low}$ , $S_4 = \text{High}$ $+3.3 V_{IN} = \text{Open Circuit}$	$T_A = 25^\circ\text{C}$		1	$\mu\text{A}$	
			$T_A = 85^\circ\text{C}$		10		
Rise Time	$t_{SW3(\text{on})}$	$S_1 = S_2 = S_4 = \text{Low}$ , See Figure 2.		0.1	1.7	ms	
Fall Time	$t_{SW3(\text{off})}$			3	30		50
<b>Switch 4</b>							
On-Resistance	$R_{ON}$	$I = 500\text{mA}$ , $S_4 = \text{High}$ $S_1 = S_2 = S_3 = \text{Low}$	$T_A = 25^\circ\text{C}$		50	m $\Omega$	
			$T_A = 85^\circ\text{C}$		70		
Off Current ( $+3.3 V_{IN}$ )	$I_{OFF}$	$+3.3 V_{IN} = 3.6 \text{ V}$ , $S_1 = S_2 = S_3 = S_4 = \text{Low}$	$T_A = 25^\circ\text{C}$		1	$\mu\text{A}$	
			$T_A = 85^\circ\text{C}$		10		
Rise Time	$t_{SW4(\text{on})}$	$S_1 = S_2 = S_3 = \text{Low}$ , See Figure 2.		0.1	0.9	ms	
Fall Time	$t_{SW4(\text{off})}$			3	20		40
<b>Switch 5</b>							
On-Resistance	$R_{ON}$	$I = 2 \text{ mA}$ , $S_1 = S_2 = \text{Low}$	$T_A = 25^\circ\text{C}$		235	400	$\Omega$
			$T_A = 85^\circ\text{C}$		325	550	
<b>Switch 6</b>							
On-Resistance	$R_{ON}$	$I = 2 \text{ mA}$ , $S_3 = S_4 = \text{Low}$	$T_A = 25^\circ\text{C}$		140	400	$\Omega$
			$T_A = 85^\circ\text{C}$		200	500	
<b>Power Supply</b>							
$+5 V_{IN}$ Current Input (on)	$I_{+5VIN(1)}$	$S_1 = S_4 = 0 \text{ V}$ , $S_2 = S_3 = 3 \text{ V}$			20	50	$\mu\text{A}$
	$I_{+5VIN(2)}$	$S_1 = S_4 = 3 \text{ V}$ , $S_2 = S_3 = 0 \text{ V}$			20	50	
$+5 V_{IN}$ Current Input (off)	$I_{+5VIN(3)}$	$S_1 = S_2 = S_3 = S_4 = 0 \text{ V}$			<1	10	
<b>Switch Control Inputs</b>							
Input Voltage High	$V_{I(H)}$	$+5 V_{IN} = 5.5 \text{ V}$	2.2	1.8		V	
		$+5 V_{IN} = 4.5 \text{ V}$	2.2	1.6			
Input Voltage Low	$V_{I(L)}$	$+5 V_{IN} = 5.5 \text{ V}$		1.6	0.8	V	
		$+5 V_{IN} = 4.5 \text{ V}$		1.4	0.8		
Input Current High	$I_{I(H)}$	$S_1$ through $S_4 = 5 \text{ V}$			1.0	$\mu\text{A}$	
Input Current Low	$I_{I(L)}$	$S_1$ through $S_4 = \text{GND}$	-1.0				

Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**TIMING WAVEFORMS**

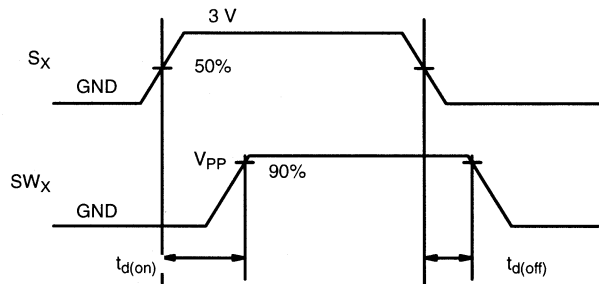


FIGURE 1.  $V_{PP}$  Switch Delay

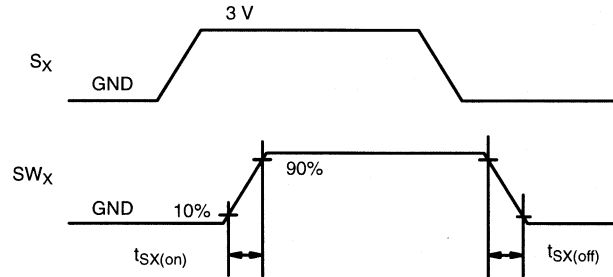


FIGURE 2. Switch Ramp

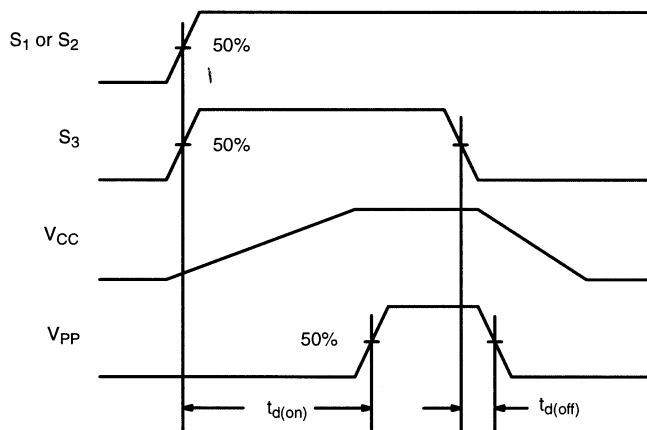
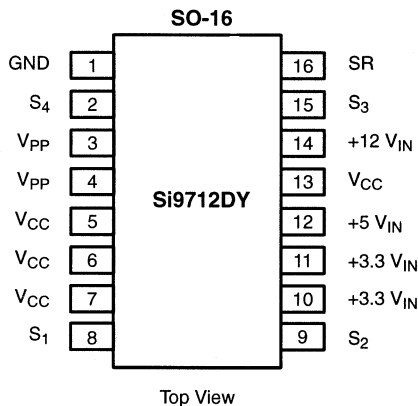


FIGURE 3. Delay from  $S_1$  or  $S_2$  to  $V_{PP}$  Power-up

**PIN CONFIGURATION**



Note:

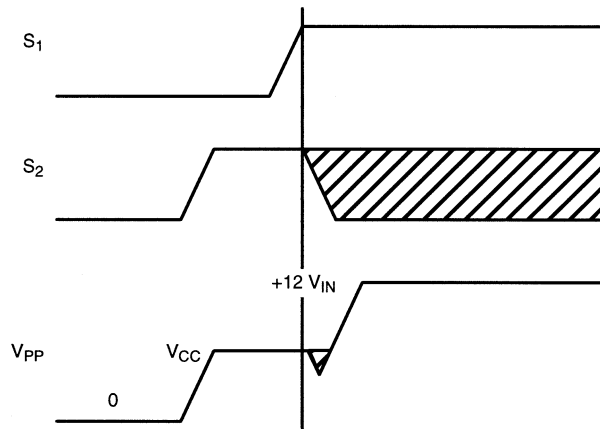
a. Pins 5, 6, 7, and 13 must be connected in the PCB for correct operation.

PIN DESCRIPTION		
Pin Number	Function	Description
1	GND	Ground connection.
2	$S_4$	Control input for selecting +3.3 $V_{IN}$ to $V_{CC}$ . The PC Card terminology for this pin is $V_{CC\_EN0}$ .
3, 4	$V_{PP}$	Program and peripheral voltage to PC Card slot.
5, 6, 7, 13	$V_{CC}$	Supply voltage to slot.
8	$S_1$	Control input for selecting +12 $V_{IN}$ to $V_{PP}$ . The PC Card terminology for this pin is $V_{PP\_EN1}$ .
9	$S_2$	Control input for selecting $V_{CC}$ to $V_{PP}$ . The PC Card terminology for this pin is $V_{PP\_EN0}$ .
10, 11	+3.3 $V_{IN}$	+3.3-V supply.
12	+5 $V_{IN}$	+5-V supply.
14	+12 $V_{IN}$	+12-V supply.
15	$S_3$	Control input for selecting +5 $V_{IN}$ to $V_{CC}$ . The PC Card terminology for this pin is $V_{CC\_EN1}$ .
16	SR	Slew rate control pin, capacitor to GND defines programmable ramp time.

<b>TRUTH TABLE<sup>b</sup></b>									
<b>S<sub>1</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>3</sub></b>	<b>S<sub>4</sub></b>	<b>Switch 1</b>	<b>Switch 2</b>	<b>Switch 3</b>	<b>Switch 4</b>	<b>Switch 5</b>	<b>Switch 6</b>
0	0	0	0	Off	Off	Off	Off	On	On
0	0	0	1	Off	Off	Off	On	On	Off
0	0	1	0	Off	Off	On	Off	On	Off
0	0	1	1	Off	Off	Off	Off	On	On
0	1	0	0	Off	Off	Off	Off	On	On
0	1	0	1	Off	On	Off	On	Off	Off
0	1	1	0	Off	On	On	Off	Off	Off
0	1	1	1	Off	Off	Off	Off	On	On
1	0	0	0	Off	Off	Off	Off	On	On
1	0	0	1	On	Off	Off	On	Off	Off
1	0	1	0	On	Off	On	Off	Off	Off
1	0	1	1	Off	Off	Off	Off	On	On
1	1	0	0	Off	Off	Off	Off	On	On
1	1	0	1	On	Off	Off	On	Off	Off
1	1	1	0	On	Off	On	Off	Off	Off
1	1	1	1	Off	Off	Off	Off	On	On

Notes

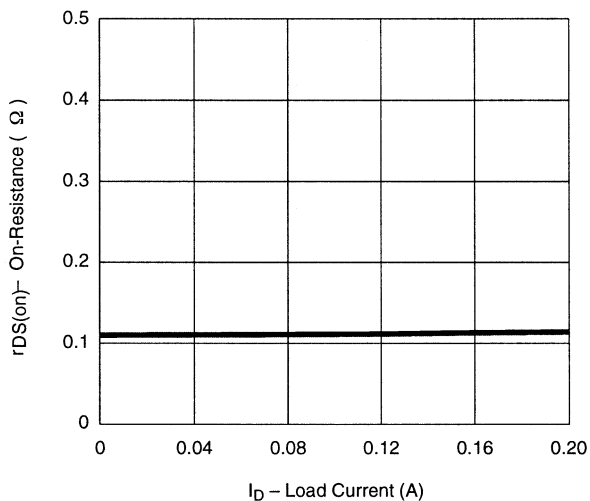
- a. Turn on of switch 1 and 2 are internally delayed until after  $V_{CC}$  is valid. See Figure 3. .
- b. Shaded lines are error conditions for PC Card applications, however, switches default to the states shown.



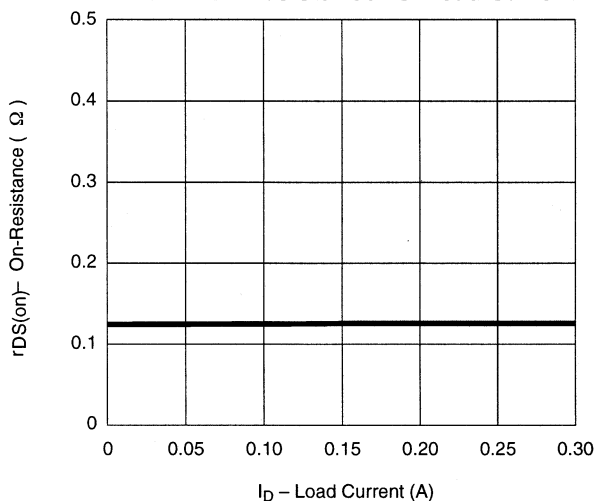
**FIGURE 4.** Break-Before-Make of SW<sub>1</sub> and SW<sub>2</sub>

**TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)**

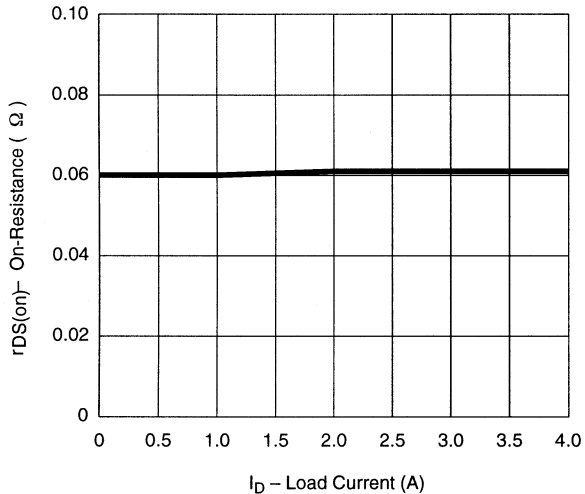
**Switch 1—On-Resistance vs. Load Current**



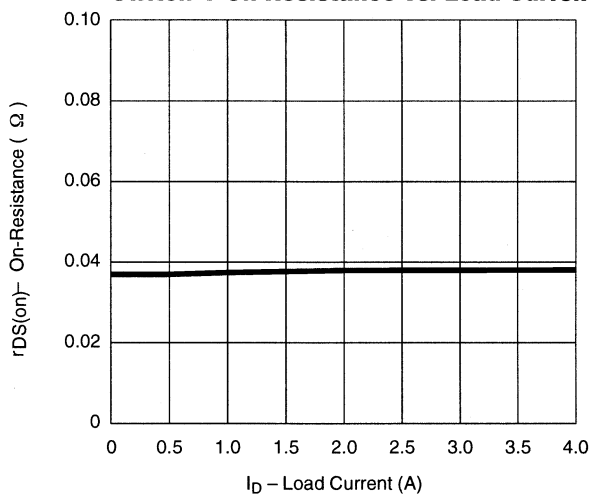
**Switch 2—On-Resistance vs. Load Current**



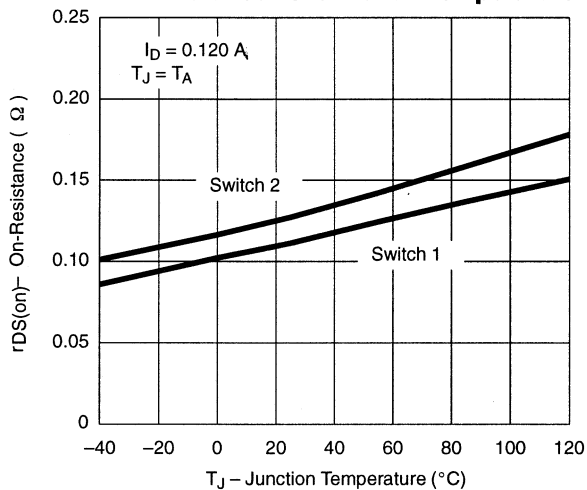
**Switch 3—On-Resistance vs. Load Current**



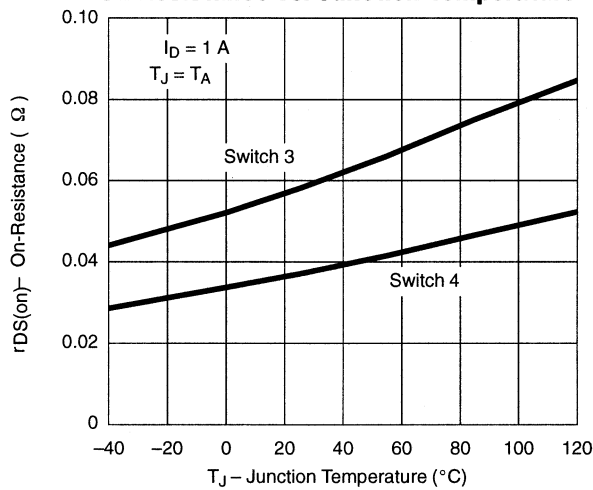
**Switch 4—On-Resistance vs. Load Current**



**On-Resistance vs. Junction Temperature**

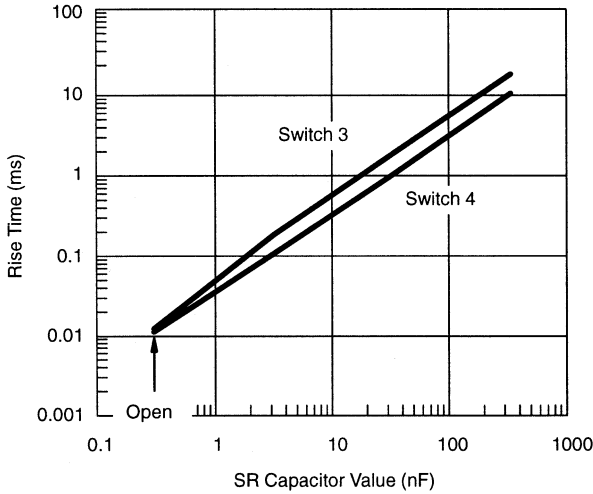


**On-Resistance vs. Junction Temperature**

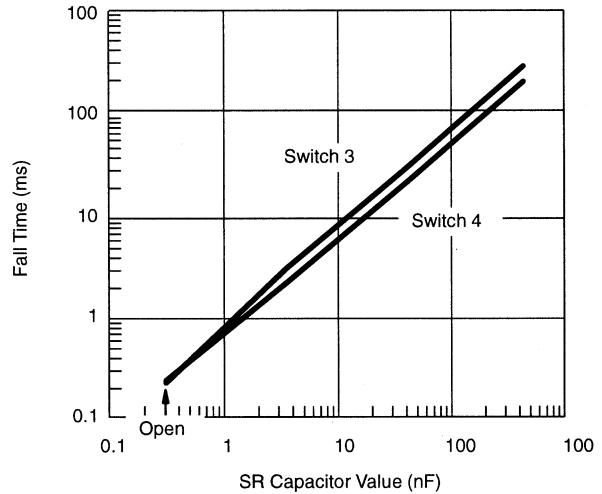


**TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)**

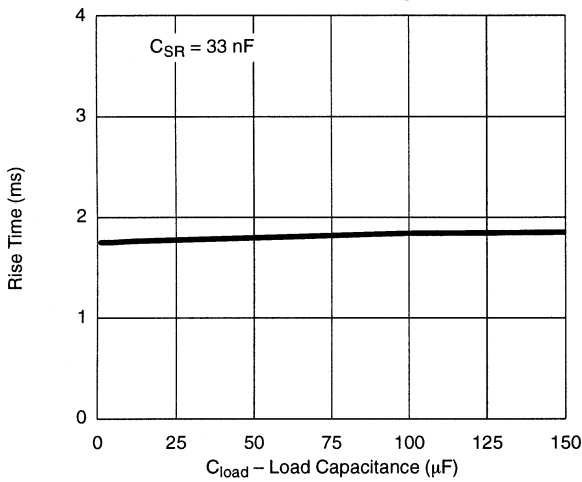
**Rise Time vs. SR Capacitor Value**



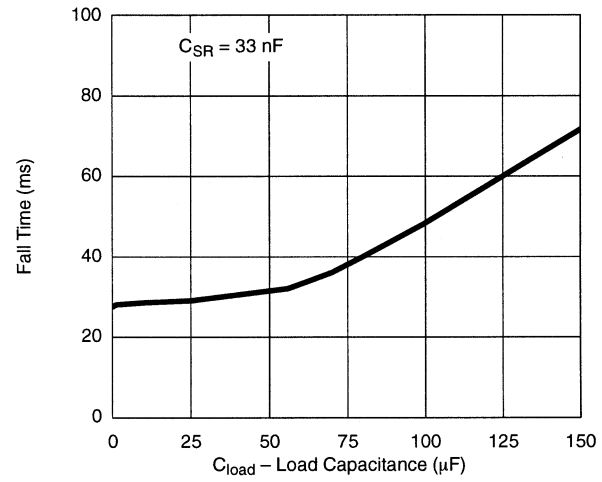
**Fall Time vs. SR Capacitor Value**



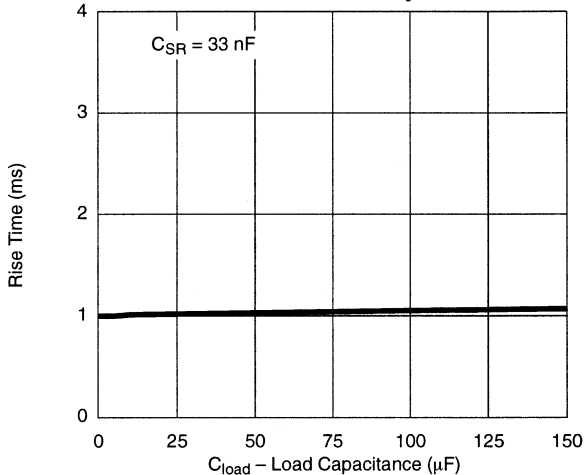
**Switch 3  
Rise Time vs. Load Capacitance**



**Switch 3  
Fall Time vs. Load Capacitance**



**Switch 4  
Rise Time vs. Load Capacitance**



**Switch 4  
Fall Time vs. Load Capacitance**

