SHARP

SPEC No. 904-1-1
ISSUE: Oct. 27, 1999

SPECIFICATIONS

Product Type: LCD Module

Model NO.: LR0G904

* This tentative specifications contains ____ pages including the cover and appendix.
If you have any objections, please contact us before you issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY Noritaki Kakoh

N. Kakoh
Dept. General Manager

REVIEWED BY: R. Shiihara

PREPARED BY: T. Shigeta

MODULE ASSEMBLY APPLICATION ENGINEERING DEPARTMENT
SYSTEMS LSI DEVELOPMENT CENTER
INTEGRATED CIRCUITS GROUP
SHARP CORPORATION

SHARP

RECORDS OF REVISION	SPEC No. 904-1-1	MODEL No. LROG904
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Oct. 27, 1999				ESTABLISHMENT	

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuing reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

● The Specifications (draft) is subject to change to improve the characteristics and performance. The examples of circuit and characteristics herein describe some typical applications. We shall not be responsible for any problem arisen from the specifications for such circuit herein and from the industrial property of any third party.

<<Notes on assembly>>

(1) The surface of polarizing plate (LCD face) of this product is easy to be damaged. Handle it with great care.
(2) If the LCD face is stained, wipe it with absorbent cotton or soft cloth. Breathe upon the LCD face and wipe it, if necessary.
(3) Water droplet on the LCD face for a long time may cause discoloration or spot. Wipe it from the face quickly.
(4) The LCD panel uses glass and is easy to be broken or chipped by dropping itself or striking it to something hard. Handle it with great care.
(5) The polarizing plate may be deteriorated by gas of epoxy resin (amine system hardening agent) and of silicon adhesive (dealcoholization system or oxime system) from any material used in the set side or from packing material. Check your material and the suitability.
(6) The internal liquid crystal is solidified at any temperature lower than the rated storage temperature and this may damage the LCD panel. If a temperature exceeds the rated temperature range, the liquid crystal becomes isotropic liquid and it may not be restored to the original state.
(7) Do not use this LCD module under the direct sunlight or intensive ultraviolet ray for a long time.
(8) Never disassemble this LCD module, otherwise an error may be made in contact.
(9) This module is equipped with CMOS LSI. Pay close attention to static electricity upon handling it.

<1> Operator
If operator's clothing, shoes, gloves, etc. are insulating material (nylon, polyethylene, rubber, etc.), the operator may be charged with the static electricity. Therefore, any operator shall put on any antistatic clothes.

<2> Equipment and facility
Any equipment or tool (e.g., automatic machine, conveyor, checker, soldering iron, mat working table, container, etc.), which has a mechanism or function of friction or peeling, may be charged with the static electricity. Therefore, any static electricity countermeasure (electrostatic grounding: 1 x 108 Ω) shall be taken to such equipment or tool.

<3> Floor
Floor fills a very important role to discharge the static electricity generated by an operator, equipment or facility. If the floor is insulating material (high polymer, rubber, etc.), the static electricity generated by an operator, equipment or facility on such insulating floor may be charged. Therefore, any static electricity countermeasure (electrostatic grounding: 1 x 108 Ω) shall be taken to such floor.

<4> Humidity
The humidity in every working site decreases the surface resistance of electrostatic material and it has a close relation to the prevention of static electricity. When the humidity becomes less than 50%, electrostatic grounding resistance of the entire material increases and electrostatic charge is promoted. Please keep the humidity 50% or more.

<5> Physical distribution
Any storage material such as container and styrene foam may be charged with the static electricity by friction or peeling upon transportation or storage and, moreover, induction charging may be caused by the static electricity with which an operator is charged. Therefore, any static electricity countermeasure shall be also taken to such storage material.

<6> Others

This LCD module is laminated to protect the screen surface from flaw, stain and dust. Upon peeling the laminating sheet, use an antistatic blower and peel it slowly. Install the antistatic blower in an assembly line to prevent the static electricity impressing to the LCD module.

(10) A display is easy to be affected by mechanical stress and the color is changed easily by slight stress. Therefore, upon installing the module in a set, fix it in the same plane so that the stress such as bending and twisting cannot be imposed to the module. To protect the front polarizing plate, set a clear acrylic plate or any other protection panel. Design taking into consideration the clearance and the strength of protection plate so that such protection plate cannot contact the display surface.

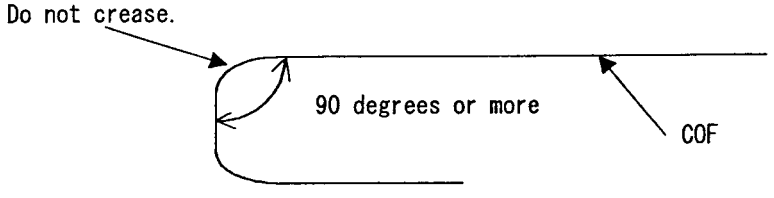
(11) If the LCD/COF connection is touched carelessly by something, contact may become incomplete. Handle it with great care.

(12) An organic material is used for the LCD/COF connection. If the organic material is applied to this part, a trouble may be made. Take care not to apply any organic solvent to this part. Take care not to touch it with a dirty hand.

(13) Upon carrying the LCD module, put it on a tray to prevent an impact to a connection of the LCD module. Any conductive tray is recommended for the prevention against the static electricity to CMOS-LSI. Upon carrying the module, grasp a glass part so that any excessive force cannot be imposed to the connection/COF.

(14) Upon assembling the module, bend so that any peeling stress cannot be imposed to LCD/COF.

(15) COF has flexibility. However, if it is creased, any trouble may be made. Upon bending it, bend it to 90 degrees or more.



(16) Because a pattern of FPC may be cut on an edge of LCD terminal, take care not to press it with materials such as a silicon rubber spacer.

(17) To prevent the COF terminal being cut after soldering to main board, it is recommended to fix COF and the board with any thin double-sided adhesive tape.

<<Notes on operation>>

(1) An operation exceeding a specified voltage may cause a trouble in this module. Be sure to use the module in a rated voltage.

(2) If any DC voltage is impressed to this module, the liquid crystal may be deteriorated. Be sure to drive it with the AC power supply.

<<Notes on storage>>
(1) Do not leave this module under the direct sunlight or intensive ultraviolet ray for a long time. Store this module in a dark place.
(2) The liquid crystal material is solidified at any temperature lower than the rated storage temperature. If a temperature exceeds the rated temperature, the liquid crystal becomes isotropic liquid and it may not be restored to the original state. The intensive humidity damages the polarizing plate. Keep the module at a normal temperature and at a normal humidity.
(3) Upon handling the module, grasp a glass part so that any excessive force cannot be imposed to the connection/part and COF.

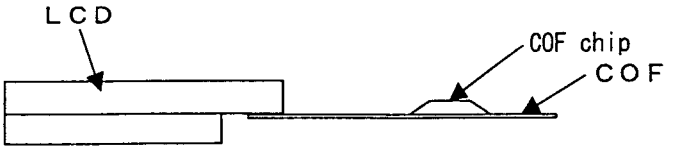
<<Notes on scrapping liquid crystal module>>
COF: Peel COF from the liquid crystal panel and treat it similarly to scrapping the circuits and boards of electronic devices.
LCD panel: Scrap as waste glass.

This LCD module contains no toxic substance. The liquid crystal panel contains no dangerous material nor toxic substance.

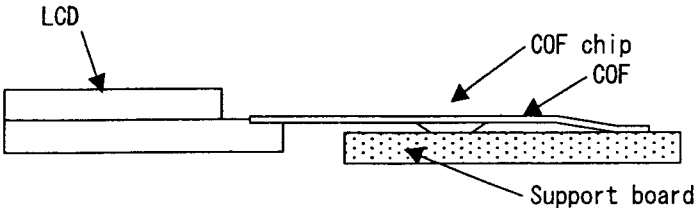
<<Any other notes>>

(1) Any specific bromine incombustible material is not used in this module.
(2) This module is not applicable to the strategic materials (or service) prescribed in the Foreign Exchange and Foreign Trade Control Law.
(3) This module contains no ozone depletion material.

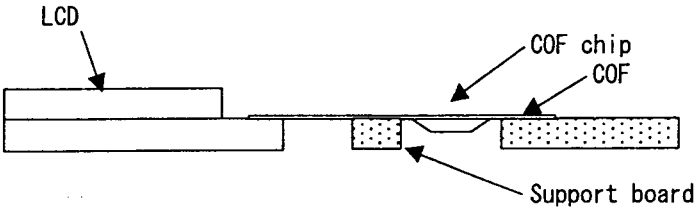
(4) Do not shine a beam of light directly at a chip face of COF.



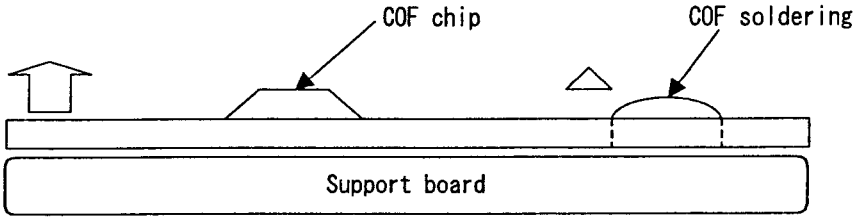
(5) If the COF chip face contacts a support board, the stress is imposed to the COF chip and any trouble may be made in COF. Take care not to impose any stress to the chip.



Upon mounting as shown above, the stress is imposed to the COF chip.
Design it so that any stress cannot be imposed to the chip as shown below.



(6) Any stress imposed to the COF soldering part may damage COF wiring. Upon soldering COFor installing, take care not to impose any stress to the COF terminal.



(7) COF chip face (substrate side) has electric potential. Do not touch any pattern on the board.

<<Handling of Defective Product >>

Warranty period of LR0G904 is one year after air way bill date of production parts at Sharp Corporation
Japan.

If defects of LR0G904 are found within warranty period during customer's manufacturing process, by Sharp's confirmation of its failure caused by Sharp manufacturing on returned LR0G904 for failure analysis, Sharp will provide replacements to customer, or guarantee costs equal to production parts of LR0G904 .

If defects of LR0G904 are found after warranty period during customer's manufacturing process or market place, by Sharp's confirmation of its failure caused by Sharp manufacturing on returned LR0G904 for failure analysis, Sharp will provider replacements at charge upon customer's request within one year after air waybill date of production parts at Sharp Corporation Japan for last time order for LR0G904 specified by customer (If customer will not place an order for LR0G904 for 6 months, customer's latest order for LR0G904 is regarded as the order for last time buy).

If epidemic failure of LR0G904 are found after warranty period during customer's manufacturing process or
market place, by Sharp's confirmation of its failure caused by Sharp manufacturing on returned LR0G904 for failure analysis, Sharp will provider replacements to customer, or guarantee costs equal to production parts
of LR0G904 .

Definition of epidemic failure is that the same kind of failure occurred by same cause will be found for
production parts of LR0G904. If 5% or over of defective parts are found in each production lot, after
Sharp's investigation, customer and Sharp regard that epidemic failure is occurred in LR0G904 production lots.

Contents

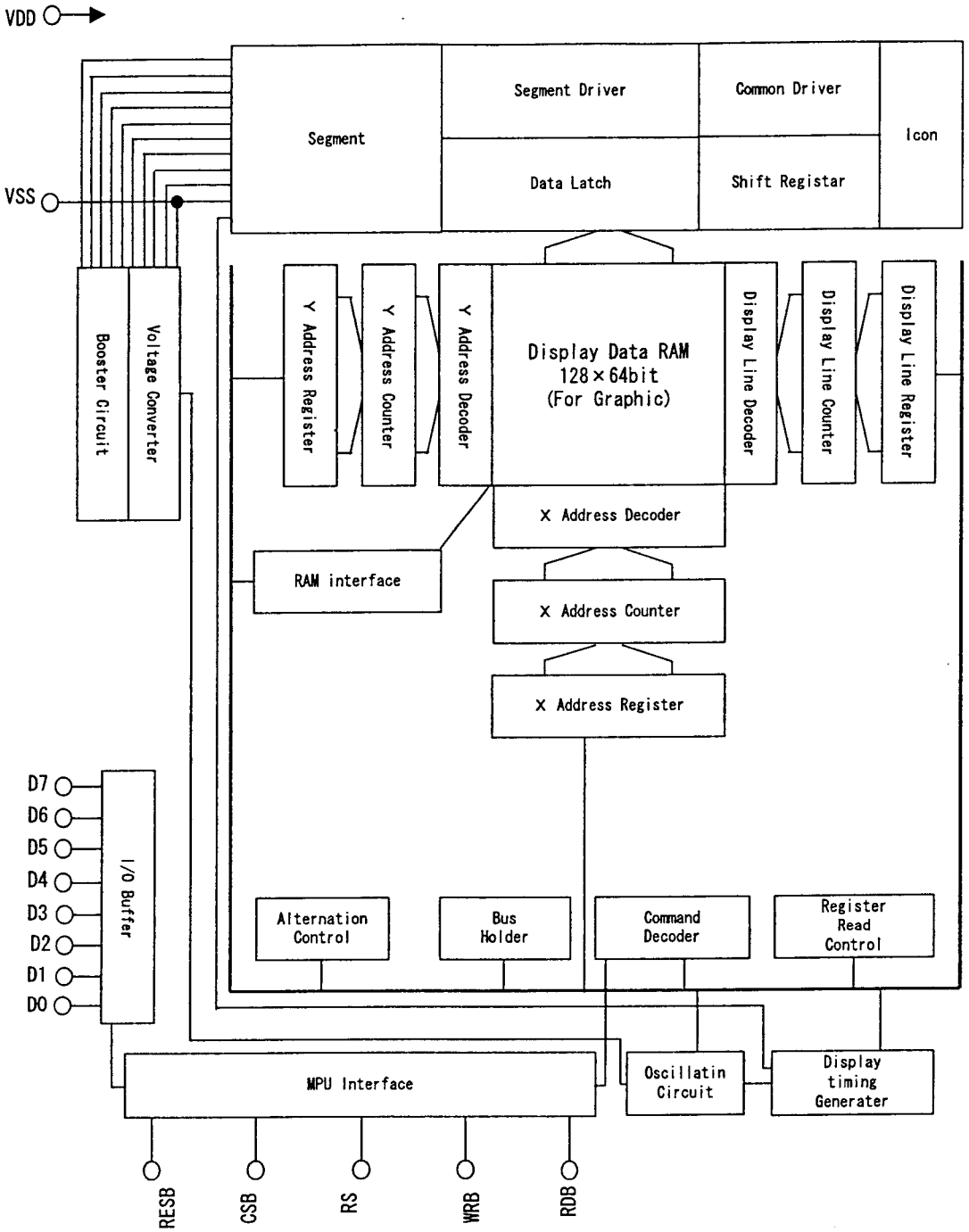
1. Summary

The LR0G904 is a dot-matrix type LCD module which uses a dot matrix LCD driver built-in RAM, which can be directly connected to a microcomputer via a bus.
8 bit parallel display data sent by a microcomputer is used to generate LCD drive signals.
Incorporating the LCD driver which features a bit-map type LCD driver that one bit of data in the Display RAM corresponds to one bit in the LCD, a lot of freedom in displaying can be accomplished.
The LR0G904 has 128 output pins for a segment driver circuit and 64 output pins for a common driver circuit in a single chip.

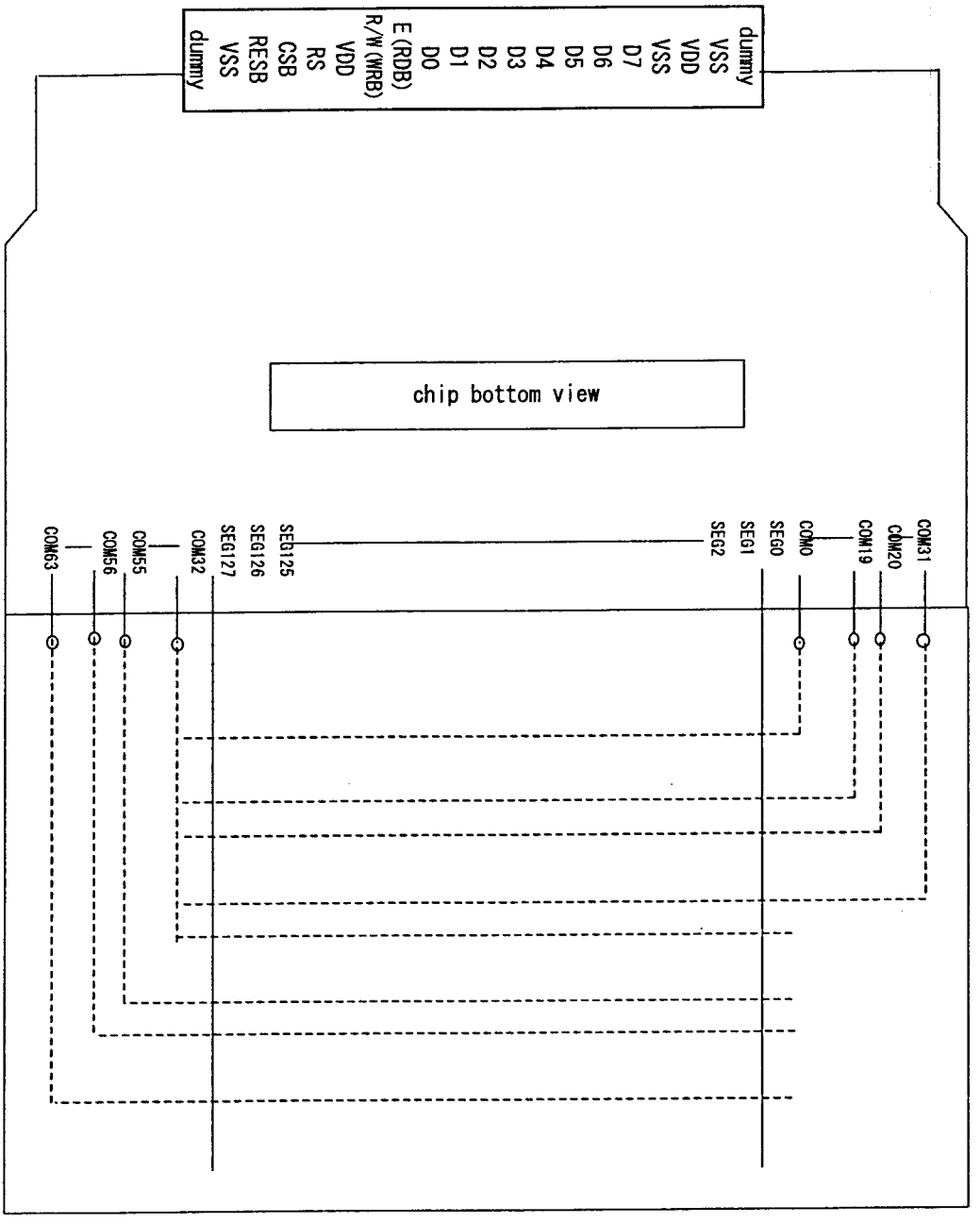
2. Features

- Graphic Display output pin 128 × 64 pins
- LCD indication by Graphic Display RAM
  - Normal Mode: RAM data "0"->not lighted, RAM data "1"->lighted
  - Reverse Mode: RAM data "1"->not lighted, RAM data "0"->lighted
- Display RAM memory capacity: 128 X 64 = 8192 bits (For graphic Display)
- 8 bit MPU interface: possible to connect 68 family MPU directly to bus line.
- Display duty ratio: 1/64
- Command features
  - Display data Read/Write
  - Setting up display starting-line :per line
  - Display ON/OFF
  - Normal/reverse display control
  - Increment control of Display RAM address
  - Write control of read modifying
  - Internal register read
  - Power saving mode
- Built-in LCD drive power circuit
  - Built-in Booster circuit: Enables four times higher voltage
  - Built-in voltage conversion circuit: Generates LCD drive voltages (V0, V1, V2, V3, or V4) based on stepped-up voltage.
  - Bias ratio of built-in power source: 1/7
  - Built-in electronic control: Controllable in 16 steps
- Power source: Supply voltage for logic system: +2.9 V to +3.1 V
  LCD drive voltage: +8.0 V to +12.0 V
- Operating temperature: -15 to +60 °C
- Packaging: LCD-module
- CMOS silicon gate process (p-type silicon circuit substrate) is used for Driver chip
- Not designed or rated as radiation hardened

3. Block Diagram



4. Pin Configuration



Note: This layout does not restrict the outer dimensions of the COF.

5. Pin Description

5-1. Input pins

Symbol	I/O	Pin Description
RESB	I	Used to reset the LR0G904. The LR0G904 is reset when "L" is entered.
CSB	I	Used to enter chip select signal. Normally,addrress bus signal is decoded and then entered.
RS	I	Used to identify data sent by MPU at D0 to D7
E (RDB)	I	Used to connect enable clock E signal for 68-family MPU. When this signal becomes "H" , LR0G904 is made active.
R/W (WRB)	I	Used to connect read/write control signal for 68-family MPU. R/W="H" : READ R/W="L" : WRITE
D0 to D7	I/O	Used as an 8-bit bidirectional data bus, which is connected to data bus in 8-bit MPU

5-2. Power supply pins

Symbol	I/O	Pin Description
VDD	Power source	Used as logic system power pin,which must be connected to +2.9 to +3.1V.
VSS	Power source	Used as ground pin,which must be connected to 0 V.

5-3. Flex Cable

The Input pins, and Power supply pins are on the surface of COF flex cable end. There is a reinforcing tab on the backside of the connector pads for securing the flex circuit into the ZIF style connector.

6. Function Description

6-1. MPU Interface

6-1-1. Interface Type

The LR0G904 performs data transfer through via the 8-bit parallel I/O(DO to d7).

I/F type	CSB	RS	RDB	WRB	Data
Parallel	CSB	RS	RDB	WRB	D0 to D7

6-1-2. Parallel Input

The LR0G904 allows parallel data transfer by connecting the data bus to an 8-bit MPU.

this 8-bit MPU used the 68-family MPU type interface .

MPU type	CSB	RS	RDB	WRB	Data
68-family MPU	CSB	RS	E	R/W	D0 to D7

6-1-3. Data Identification

The LR0G904 identifies the data types over the 8-bit data bus by combinations of RS and R/W signals.

RS	R/W	FUNCTION
1	1	Read internal register
1	0	Write internal register
0	1	Read display data
0	0	Write display data

6-2. Access to Display RAM and Internal Register

The LR0G904 makes access to Display RAM, and internal register by data bus D0 to D7, chip select CSB pin, Display RAM/register shifting RS pin, and read/write control RDB and WRB pins.

When CSB is at "H", it is in non-selective state and cannot make access to Display RAM and internal registers. In making access to them, set CSB to "L".

The access to either Display RAM or internal registers can be shifted by RS input.

RS="L" : Display RAM data

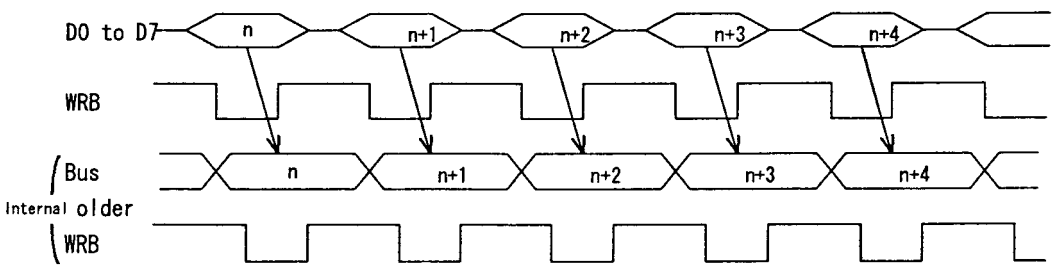
RS="H" : Internal command register

The data of 8-bit data bus D0 to D7 are written by write-operation after address setting through MPU. The timing of Write is at the falling of E.

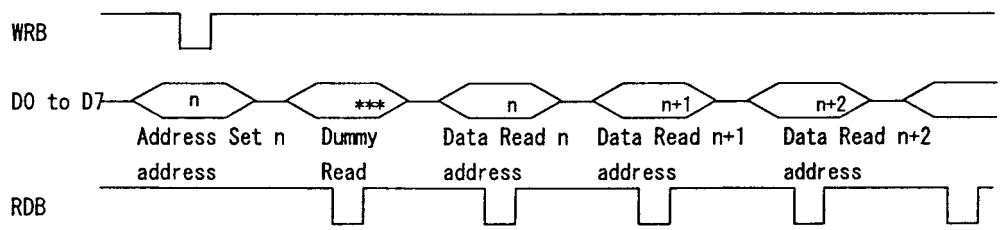
Write is internally processed by placing intermediately the bus holder in the internal data bus. In case of writing data from MPU, the data are temporally held in the bus holder before they are written by the time of the next cycle . Since the Read sequence of Display RAM data is limited, note that when Address Set is made, the designated address data are not output to Read Command immediately after the Address Set, but are output when the second data Read, resulting in requiring dummy Read one time.

Dummy Read is always required one time after Address Set and Write Cycle.

Data Write Operation

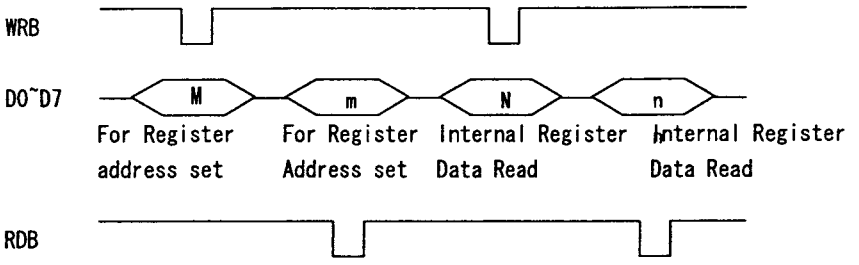


Data Read Operation



6-3. Read of Internal Register

The LR0G904 reads not only Display RAM, but also the internal registers. Addresses for Read (0, 2 to E[hex]) are allotted to each internal register. In reading the internal registers, the addresses of internal registers allotted to read are written in the registers for internal register Read and then are read.



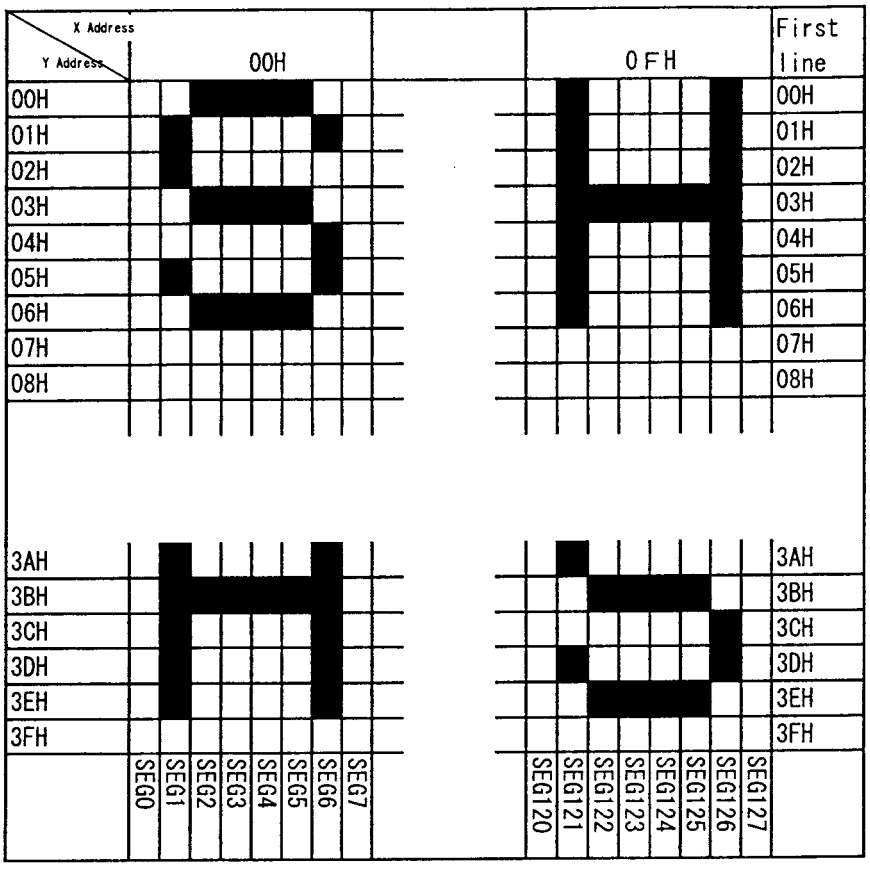
6-4. Display Mode (Graphic Display mode)

This mode enables 64 × 128 Built-in SRAM and 64 common × 128 segment output terminal.

Graphic Display's Memory map is below.

The Memory for Graphic Display is accessed by 8 bits at one time.

X address is from 00H to 0FH and Y address is from 00H to 3FH.



6-5. Display Starting Line Register

This register is for determining display start line (usually the most upper line) corresponding to COM0 in case of displaying the Display data RAM.
The register is also used in picture-scrolling.
The 6-bit display starting address is set in this register by display starting-line setting command.

6-6. Addressing of Display RAM

Display RAM consists of 128 × 64 bits memory, and makes access in 8 bit unit to an address specified by X address and Y address from MPU.
The addresses, X and Y are possible to be set up so that they can increment automatically with the address control register. The increment is made every time Display RAM is read or written from MPU. (See Command Function.)
Though the X direction side is selected by X address while the Y direction side by Y address, 10H-FFH in the X address are inhibited and do not have the X address set in these addresses.
43FH-FFH in the Y address are inhibited and do not have the Y address set in these addresses.

6-7. Display RAM Data and LCD

One bit of Display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

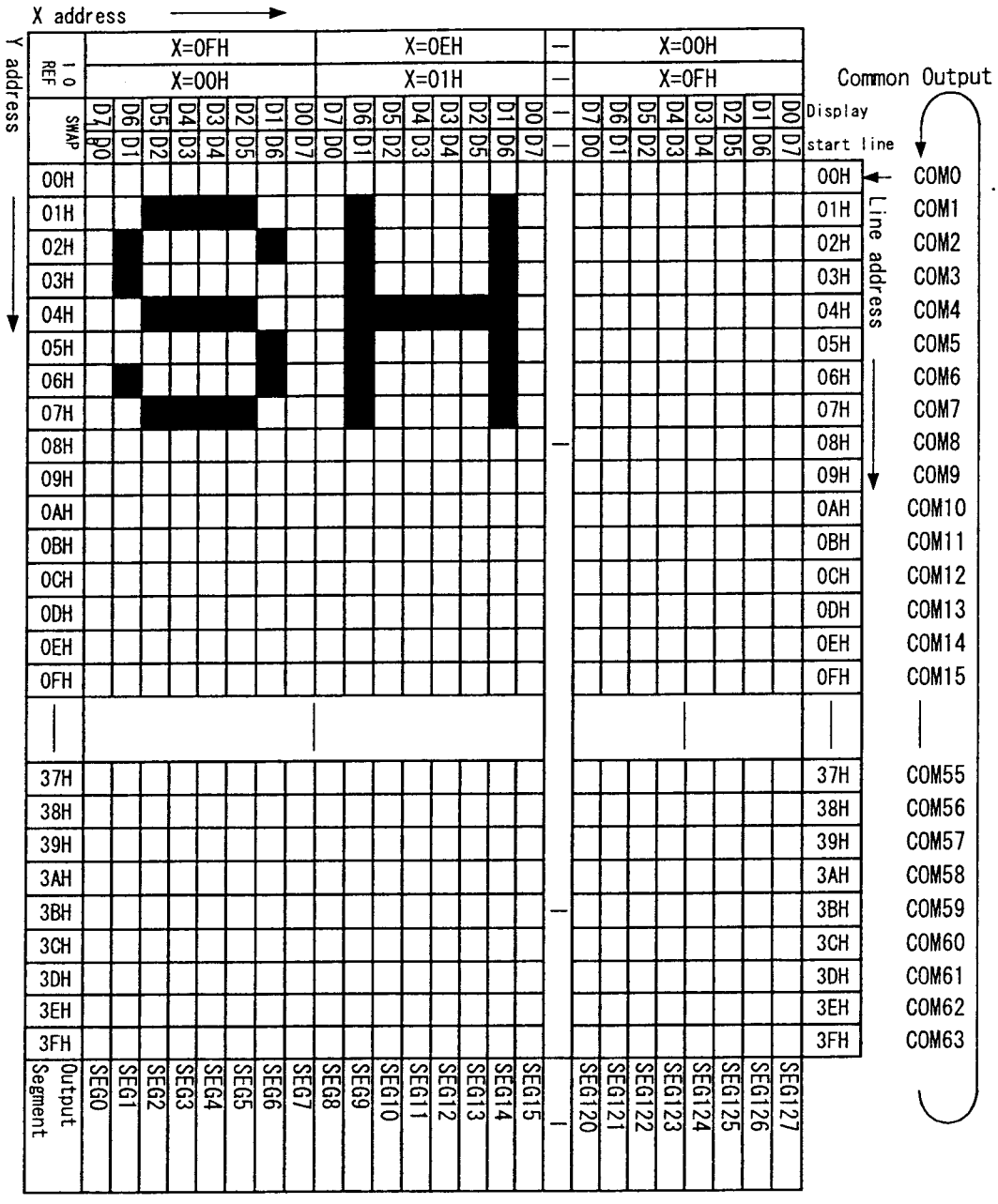
- Normal display (REV=0) : RAM data="0" not lighted
  RAM data="1" lighted
- Reverse display (REV=1) : RAM data="0" lighted
  RAM data="1" not lighted

6-8. Segment Display Output Order/Reverse Set Up

The order of display outputs, SEG0 to SEG127 can be reversed by reversing access to Display RAM from MPU by using REF register.

6-9. Relationship between Display RAM and Address

(Configuration of Display Starting Line Address "00H")



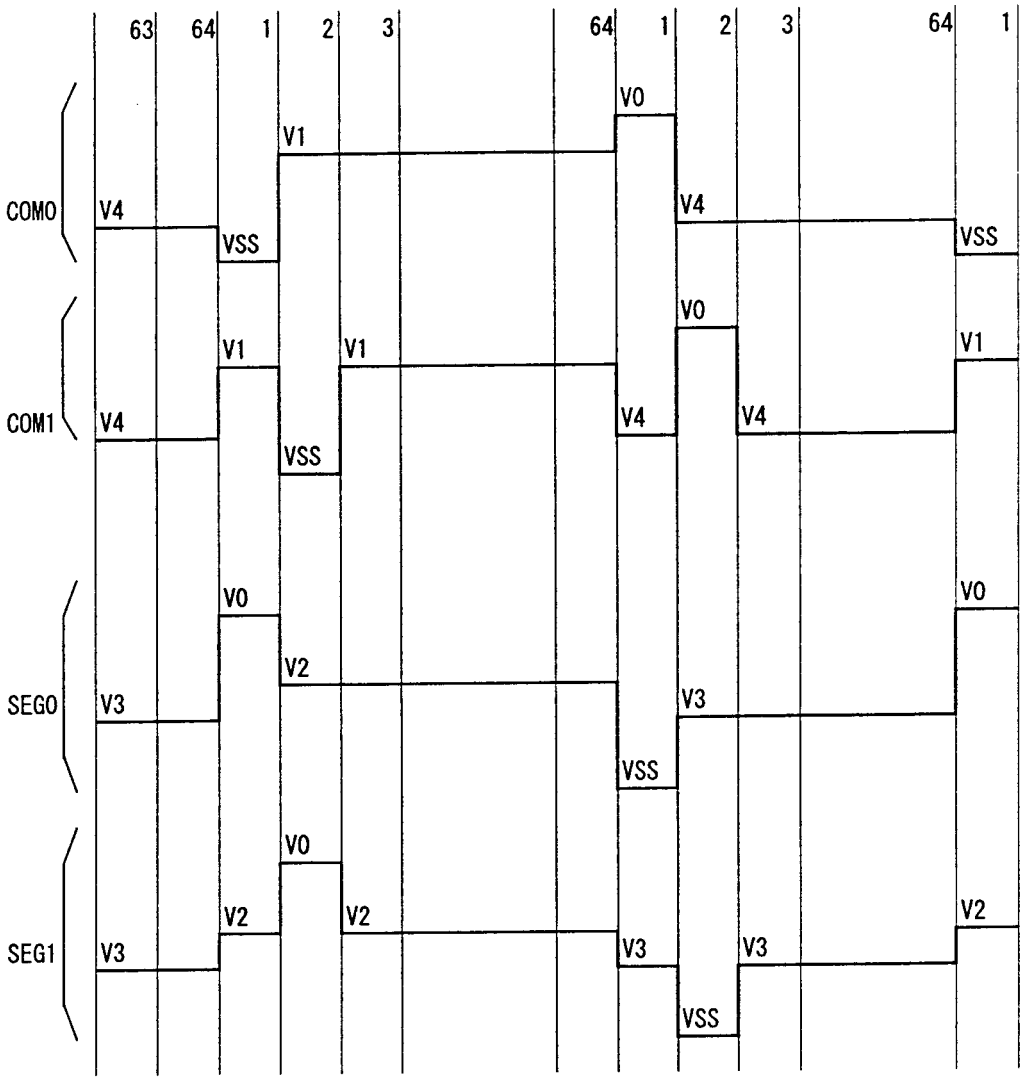
6-10. Display Data Latching Circuit

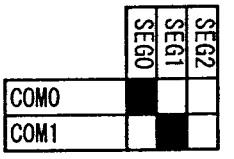
Display Data Latching Circuit temporary latches display data that is output display data to LCD driver circuit from Display RAM every one common period.

Normal display/reverse display, display ON/OFF, and display all on command are operated by controlling data in the latch. And no data within Display RAM changes.

6-11. Output Timing of LCD Driver

Display timing at Normal mode





6-12. Oscillating Circuit

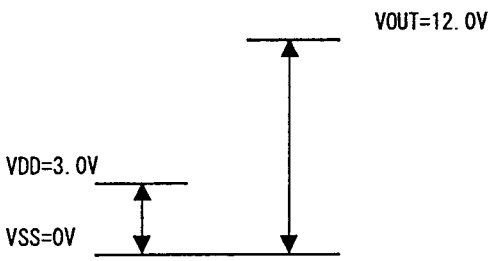
The frequency of this CR oscillator is controlled by the feedback resistor Rf.
The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster.

6-13. Power Supply Circuit

This circuit supplies voltages necessary to drive LCD panel.
The circuit consists of booster and voltage converter.
Boosted voltage from the booster is fed to the voltage converter which converts this high input voltage into V0, V1, V2, V3 and V4

6-14. Booster Circuit

VDD and VSS boosted four times.
The boosted voltage is output to VOUT pin.



When boosted Four Times

6-15. Electronic Control

The voltage conversion circuit incorporates an electronic control, which allows the LCD drive voltage level V0 to be controlled with a command and also allows the tone of LCD display to be controlled.

If 4-bit data is stored in the register of the electronic control, one level can be selected among 16 voltage values for the LCD drive voltage V0.

6-16. LCD Drive Voltage Generation Circuit

The voltage conversion circuit incorporates a voltage generation circuit, which divides the electric potential at the V0 pin with resistors to generate the electric potentials V0, V1, V2, V3 and V4 which are required for LCD drive.

6-17. Initialization

The LR0G904 is initialized by setting RESB pin at "L".

Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU.

When power ON, be sure to make reset operation.

ITEM	INITIAL STATE
Display RAM	not fixed
X-address	00H set
Y-address	00H set
Display starting line set	at the first line (0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/64
Common shift direction	COM0 -> COM63
Increment mode	Increment OFF
REF mode	Normal
Data SWAP Mode	Data SWAP Mode OFF
electronic volume	(1,1,1,1)
Power Supply	OFF

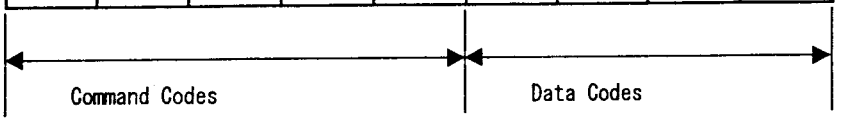
7. Command Function

The LR0G904 has a lot of commands as shown in a list of command and each command is explained in detail as follows.

Data codes and command codes are defined as follows and the execution of commands must be made in the state of chip select (CSB="L").

(For example X address)

RS	D7	D6	D5	D4	D3	D2	D1	D0
1※	0	0	0	0	AX3	AX2	AX1	AX0



The undefined command codes are inhibited.

7-1. Data Write to Display RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Display RAM write data							

The Display RAM data of 8-bit are written in the designated X and Y address.

7-2. Data Read to Display RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Display RAM read data							

The 8-bit contents of Display RAM designated in X and Y address and read out. Immediately after data are set in X and Y address, dummy read is necessary once.

7-3. X Address Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	AX3	AX2	AX1	AX0

(At the time of reset: AX3 to AX0 =0H, read address : 0H)

Addresses of Display RAM's X direction are set. The values of AX3 to AX0 are usable up to 00H-0FH , but 10H-FFH are inhibited. When the register setting SEG output normal/reverse is REF = "0", the data of AX3 to AX0 are addressed to Display RAM as they are.

When REF = "1", the data of 0FH-(AX3 to AX0)H are addressed to Display RAM.

7-4. Y Address Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	AY3	AY2	AY1	AY0

(At the time of rest : AY3 to AY0 = 0H, read address: 2H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	※	AY6	AY5	AY4

※ mark shows "Don't care" (At the time of reset : AY6 to AY4 = 0H , read address : 3H)

Addresses of Display RAM's Y direction are set. In data setting, lower place and upper place are divided with 4 bit and 3 bit respectively.

When data set, lower place must be set first and upper place must be set second.

The values of AY6 to AY0 are usable up to 00H-42H , but 43H-FFH are inhibited.

7-5. Display Starting Line Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	LA3	LA2	LA1	LA0

(At the time of reset : LA3 to LA0 = 0H , read address : 4H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	※	※	LA5	LA4

※ mark shows "Don't care" (At the time of reset : LA4, LA5 = 0H , read address :5H)

The display line address is required to designate, and the designated address becomes the display line of COM0.

The display of LCD panel is indicated in the increment direction of the designated display starting address to the line address.

LA5	LA4	LA3	LA2	LA1	LA0	LINE ADDRESS
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		:				:
1	1	1	1	1	1	63

7-6. n Line Alternated Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	N3	N2	N1	N0

(At the time of reset : N3 to N0 = 0H , read address : 6H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	※	※	N5	N4

※ mark shows "Don't care" (At the time of reset : N5 to N4 = 0H , read address : 7H)

The reverse line number of LCD alternated drive is required to set in the register. The line number possible to set is 2-64 lines.

The values set up by the n-line alternated register become enable when the n line alternated drive command is ON. (NLIN = "1")

When the n line alternated drive command is OFF (NLIN = "0"), alternated drive waveform which reverses by frame cycle is generated.

N5	N4	N3	N2	N1	N0	REVERSE LINE NUMBER
0	0	0	0	0	0	—
0	0	0	0	0	1	2
		:				:
		:				:
1	1	1	1	1	1	64

7-7. Display Control (1) Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	SHIFT	0	ALLON	ON/OFF

(At the time of reset : (SHIFT, SEGON, ALLON, ON/OFF) = 0H, read address : 8H)

Various control of display is set up.

(i) ON/OFF Command

To control ON/OFF of the Graphic Display

ON/OFF = "0" : display OFF

ON/OFF = "1" : display ON

(ii) ALLON Command

Regardless of the data of the Graphic Display RAM, the Graphic Display are on. This command has priority over display normal/reverse commands.

ALLON = "0" : normal display

ALLON = "1" : all display lighted

(iii) SHIFT Command

The shift direction of the Graphic Display scanning data in the common driver output is selected.

SHIFT = "0" : COM0->COM63 shift-scan

SHIFT = "1" : COM63->COM0 shift-scan

7-8. Display Control (2) Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	1	REV	NLIN	SWAP	REF

(At the time of reset : (REV, NLIN, SWAP, REF) = 0H, read address : 9H)

Various control of display is set up.

(i) REF Command

When MPU accesses to the Graphic Display RAM, the relationship between X address and write data is normalized or reversed.

Therefore, the order of segment driver output can be reversed by register setting.

REF	ACCESS FROM MPU		INTERNAL ACCESS		CORRESPONDING SEG OUTPUT
	X ADDRESS	D7-D0	X ADDRESS	D7-D0	
0	NH	D0(LSB) D7(MSB)	NH	(LSB) (MSB)	SEG(8*NH)Output SEG(8*NH+7)Output
1	NH	D0(LSB) D7(MSB)	0FH-NH	(MSB) (LSB)	SEG(8*(0FH-NH)+7)Output SEG(8*(0FH-NH))Output

(ii) SWAP Command

When data to the Graphic Display RAM are written, the write data are swapped.

SWAP = "0" : Normal mode. In data-writing, the data of D7 to D0 can be written to the Graphic Display RAM.

SWAP = "1" : SWAP mode ON. In data-writing, the swapped data of D7 to D0 can be written to the Graphic Display RAM.

	SWAP="0"	SWAP="1"
EXTERNAL DATA	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0
INTERNAL DATA	d7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7

(iii) NLIN Command

The ON/OFF control of n-line alternated drive is performed.

NLIN = "0" : n line alternated drive OFF.

NLIN = "1" : n line alternated drive ON. According to data set up in n line alternated register, the alternation is made.

(iv) REV Command (For the Graphic Display only)

Corresponding to the data of the Graphic Display RAM, the lighting or not-lighting of the display is set up.

REV = "0" : When RAM data at "H", LCD at ON voltage (normal)

REV = "1" : When RAM data at "L" , LCD at ON voltage (reverse)

7-9. Increment Control Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	※	AIM	AYI	AXI

※mark show "Don't care" (At the time of reset : (AIM, AYI, AXI) = 0H, read address : AH)

The increment mode is set up when accessing to the Graphic Display RAM.

By AIM, AYI, and AXI registers, the setting-up of increment operation/non-operation for the X-address counter and the Y-address counter every write access or every read access to the Graphic Display RAM is possible.

In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to the Graphic Display RAM from MPU.

After setting this register, be sure to set the X and Y Address Register. Because it is not assuring the data of X and Y Address Register after setting Increment Control Register.

The increment control of X and Y address by AIM, AYI and AXI registers is as follows.

AIM	SELECTION OF INCREMENT TIMING	REFERENCE
0	When writing to Graphic Display RAM or reading from Graphic Display RA	<1>
1	Only when writing to Graphic Display RAM(read modify)	<2>

<1>This is effective when subsequently writing and reading the successive address area.

<2>This is effective in the case that after reading and writing the successive address area every address, the read data are modified to write.

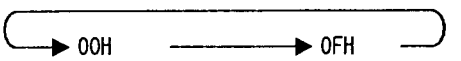
AYI	AXI	SELECTION OF INCREMENT ADDRESS	REFERENCE
0	0	Increment is not made	<1>
0	1	X address automatic increment	<2>
1	0	Y address automatic increment	<3>
1	1	X and Y address cooperative, automatic increment	<4>

<1> Regardless of AIM, no increment for X and Y address.

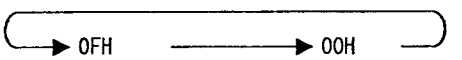
<2> According to the setting-up of AIM, increment or decrement for only X address.

In accordance with the REF conditions of SEG normal/reverse output setting register, X address becomes as follows.

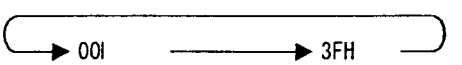
·At REF = "0" (normal output) , increment by loop of



·At REF = "1" (reverse output), decrement by loop of



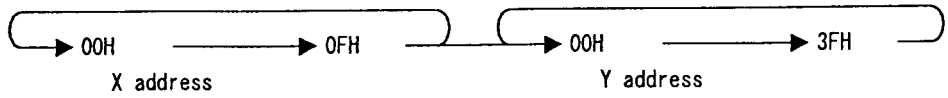
<3>According to the setting-up of AIM, increment for only Y address. Regardless of REF, increment by loop of



for Y address.

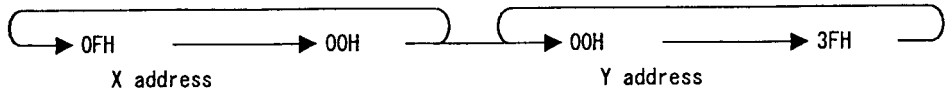
<4>According to the setting-up of AIM, cooperative variation for X and Y address.
When the access of X address is made up to 0FH, Y address increment occurs.

·At REF = "0" (normal output)



vary in the above loops.

·At REF = "1" (reverse output)



vary in the above loops.

7-10. Power Control Register Set (1)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	1	1	HALT	PON	ACL

(At the time of reset : (BIAS, HALT, PON, ACL) = 0H , read address : BH)

(1) ACL Command

The internal circuit can be initialized. This command is enabled only at Master operation mode.

ACL = "0" : Normal operation
ACL = "1" : Initialization ON

If the power control register is read out immediately after executing ACL command (ACL=1) , the D0 bit is in the state of "1" . Therefore, if the reset operation is internally started, the D0 bit becomes "0" .

In executing ACL command, the internal reset signals are internally generated by using display-clock original oscillation (oscillation by OSC1 and OSC0) .

Therefore, after executing ACL command, allow WAIT period having at least two cycle portion of the original oscillation clock before the next processing is made.

(ii) PON Command

The internal power supply for the Graphic Display circuit is set ON/OFF .

PON = "0" : Power supply for the Graphic Display circuit OFF
PON = "1" : Power supply for the Graphic Display circuit ON

At PON = "1" : the booster and voltage converter for the Graphic Display circuit function.

(iii) HALT Command

The conditions of power-saving are set ON/OFF by this command.

HALT = "0" : Normal operation
HALT = "1" : Power-saving operation

When setting in the power -saving state, the consumed current can be reduced to a value near to the standby current. The internal conditions at power-saving are as follows.

(a) The oscillating circuit and power supply circuit are stopped.
(b) The LCD drive is stopped, and outputs of the segment driver and common driver are VSS level.
(c) The contents of the Display RAM data are maintained.
(d) The operational mode maintains the state of command execution before executing power-saving command.

7-11. Power Control Register Set(2)

Electronic volume for the Graphic Display

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	MSB	·	·	· · LSB

(At the time of reset : (DVOL) = FH, read address : DH)

The LCD drive voltage V0 output from the built-in power circuit can be controlled and the display tone on the LCD can be also controlled.

The LCD drive V0 takes one out of 16 voltage values by setting 4 bit data register.

MSB	· · · ·	LSB	V0
0	0 0	0	Smaller
	·		·
	·		·
1	1 1	1	Larger

If the electronic control is not used, specify(1, 1, 1, 1) in the 4-bit data register. After the LH155K is reset, the 4-bit data register is automatically set to (1, 1, 1, 1).

7-12. Power Control register Set (3)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	DU1	DU0	BS1	BS0

(At the time of reset : (DU1, DU0, BS1, BS0) = 0H , read address : EH)

(i)BS Command

Select boost voltage level below.

BS		BOOST
BS1	BS0	VOLTAGE LEVEL
0	0	4 TIMES
0	1	3 TIMES
1	0	2 TIMES
1	1	PROHIBITION

Do not set BS1="1", BS0="1".

(ii)Duty Command

Select Duty ratio below. Please select DU1="0"and DU0="0".

DUTY		
DU1	DU0	DUTY RATIO
0	0	1/64

7-13. RE Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	1	1	1	1	※	※	※	RE

※mark shows " Don't care", (At the time of reset : (RE) = 0H, read address : FH)

RE = "1" : the extended function set, Duty ratio select and boost voltage level select can be accessed.

7-14. Address Set for Internal Register Read

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	RA3	RA2	RA1	RA0

(At the time of reset : (RA3, RA2, RA1, RA0) = BH)

Then data set up in the internal registers are read out, set the address for Read allotted to each register by this command before executing the Read command of the internal registers.
For example, when the data of the command register in the display control (1) are read out, set the values of (RA3, RA2, RA1, and RA0) = 8H.
Refer to the Function description of each command or a list of commands on the address for Read allotted to each command register.

7-15. Internal Register Read

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	※	※	※	※	Internal register read data			

※mark shows "Don't care "

Command for reading out the data of the internal registers.
When this command is executed, the address for read in the internal registers to be read must be preset.

7-16. Command Function Table

Instruction	Codes					Codes								Function
	CSB	RS	WRE	RDB	RE	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data write	0	0	0	1	0	Write Data								Write to Display RAM
Display data read	0	0	1	0	0	Read Data								Read from Display RAM
X Address set [0H]	0	1	0	1	0	0	0	0	0	X Address				Set of X direction Address in Display RAM
Y Address set (Lower) [2H]	0	1	0	1	0	0	0	1	0	Y Address				Set of Y direction Address in Display RAM
Y Address set (Upper) [3H]	0	1	0	1	0	0	0	1	1	※	Y Address			Set of Y direction Address in Display RAM
Display Starting Line Set (Lower) [4H]	0	1	0	1	0	0	1	0	0	Display Start Line				Set Line Add. of RAM Making COMO Display
Display Starting Line Set (Upper) [5H]	0	1	0	1	0	0	1	0	1	※	※	Display Start Line		Set Line Add. of RAM Making COMO Display
n Line Alternation Set (Lower) [6H]	0	1	0	1	0	0	1	1	0	Alternated Line				Set the Number of Alternated Reverse Line
n Line Alternation Set (Upper) [7H]	0	1	0	1	0	0	1	1	1	※	※	Alternated Line		Set the Number of Alternated Reverse Line
Display Control (1) [8H]	0	1	0	1	0	1	0	0	0	SHIFT	0	ALLON	ON/OFF	(1)
Display Control (2) [9H]	0	1	0	1	0	1	0	0	1	REV	NLIN	SWAP	REF	(2)
Increment Control [AH]	0	1	0	1	0	1	0	1	0	※	AIM	AYI	AXI	AIM:Increment Timing select AYI:Y incr., AXI:X Incr.
Power Control (1) [BH]	0	1	0	1	0	1	0	1	1	1	HALT	PON	ACL	HALT: Halt on/off PON:Source ON, ACL Reset
Power Control (2) [DH]	0	1	0	1	0	1	1	0	1	DVOL				Set Electronic Control
Power Control (3) [EH]	0	1	0	1	1	1	1	1	0	DUTY DU1	DUTY DU0	BS BS1	BS BS0	DUTY:Select Duty ratio BS :Select boost voltage level
RE Register [FH]	0	1	0	1	0/1	1	1	1	1	※	※	※	RE	RE Flag Setting
Address Set for Internal Register Read	0	1	0	1	0	1	1	0	0	Address for Register Read				Set Address of Internal Register for Reading
Internal Register Read	0	1	1	0	0	※	※	※	※	Read Data				Read Out Internal Register Register

(1) SHIFT : Common Shift Direction, ALLON: All ON,
ON/OFF: Graphic Display ON/OFF
(2) REV: Graphic Display Normal/Reverse, NLIN: n Line Reverse ON/OFF,
SWAP: Data for Graphic Display Swap,
REF: Segment Output for Graphic Display Normal/Reverse

8. Absolute Maximum Ratings

Rating	Symbol	Condition	Applicable Pin	Value	Unit
Supply Voltage	VDD	Ta=+25°C	VDD	- 0.3 ~ + 6.0	V
Input Voltage	VI	Referenced to VSS(0V)	*1	- 0.3 ~ VDD + 0.3	V
Storage Temperature	Tstg			- 20 ~ + 70	°C

*1 D0~D7,CSB,RS,RDB,WRB,RESB pins

9. Recommended Operating Conditions

Paramerter	Symbol	Applicable Pin	MIN	TYP	MAX	Unit	Note
Power Supply Voltage	VDD	VDD	2.9		3.1	V	*1
Operating Temperature	Topr		-15		60	°C	

*1 shows applying voltage to VSS pin.

10. Electrical Characteristics

10-1. DC Characteristics

Unless otherwise specified,VSS=0 V,VDD=+2.9 to 3.1 V,Ta=-15 to +60 °C

Paramerter	Symbol	Applicable condition	MIN.	TYP.	MAX.	Unit	Applicable pin
High-level input voltage	VIH		0.8VDD		VDD	V	*1
Low-level input voltage	VIL		0		0.2VDD	V	*1
Input leakage current	ILI	VI=VSS or	-10		10	μA	*1
Oscillating frequency	fosc	Rf=680kΩ±2% VDD=3V		28		kHz	
Consumed current(1)	IDD1	VDD=3V,Boosting 4 times		160	190	μA	*2
Consumed current(2)	IDD2	VDD=3V,Boosting 4 times		410	500	μA	*3
Module power consumption	Pd	VDD=3V,Boosting 4 times		1230	1500	μW	*3
Reset("L")pluse width	tRW	IOL=-0.4 mA	10			μs	*4

Applicable pins

*1 D0~D7,CSB,RS,RDB,WRB,RESB pins

*2 VDD pin

When the built-in oscillating circuit(Rf=680 k Ω) and built-in power supply ON(PMODE="L") are used and there is no access from MPU, this pin is applied.
Boosting four times is used. Electronic control is used(The code is"0111").
The display is all on pattern.

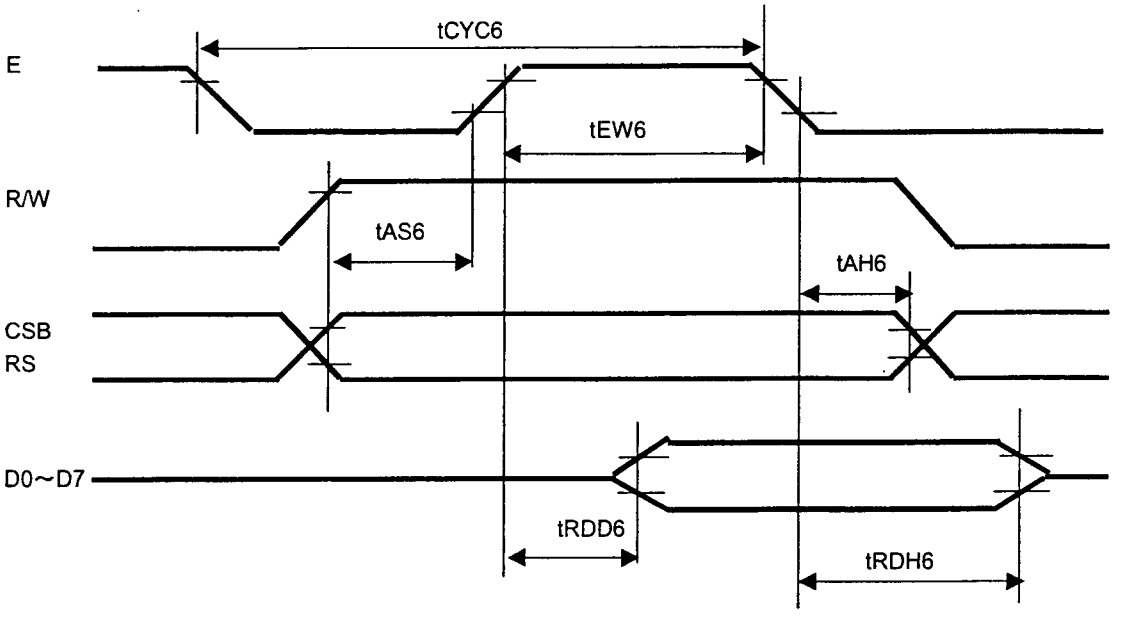
*3 VDD pin

When the built-in oscillating circuit(Rf=680 k Ω) and built-in power supply ON(PMODE="L") are used and there is no access from MPU, this pin is applied.
Boosting four times is used. Electronic control is used(The code is"0111").
The display is checker pattern.

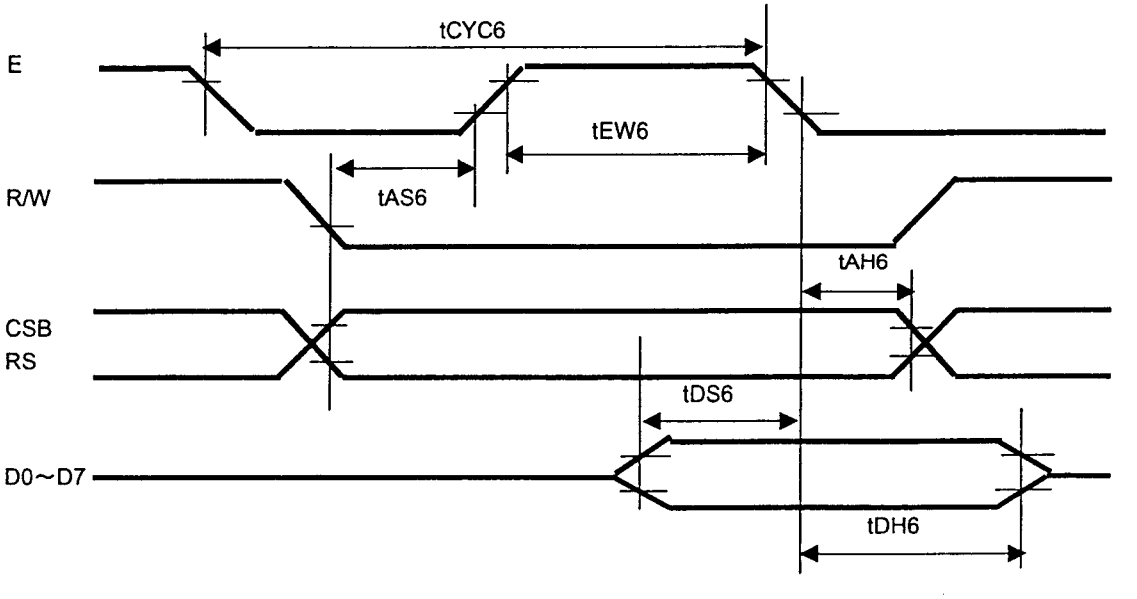
*4 RESB pin

(2) System Bus Read/Write Timing

(Read timing)



(Write timing)



(MPU timing characteristics)

(VDD=2.7～3.3 V, Ta= -15～ +60 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		18		ns	CSB
Address setup time	tAS6		0		ns	RS
System cycle time	tCYC6		400		ns	E
Enable pulse width	tEW6		250			
Read data output delay	tRDD6	CL=15 pF		220	ns	D0～D7
Read data hold time	tRDH6		10		ns	
Input signal rise and fall	tr, tf			15	ns	All of above pins

(VDD=2.4～2.7 V, Ta= -15 ～ +60 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		23		ns	CSB
Address setup time	tAS6		0		ns	RS
System cycle time	tCYC6		600		ns	E
Enable pulse width	tEW6		300			
Read data output delay	tRDD6	CL=15 pF		250	ns	D0～D7
Read data hold time	tRDH6		10		ns	
Input signal rise and fall	tr, tf			30	ns	All of above pins

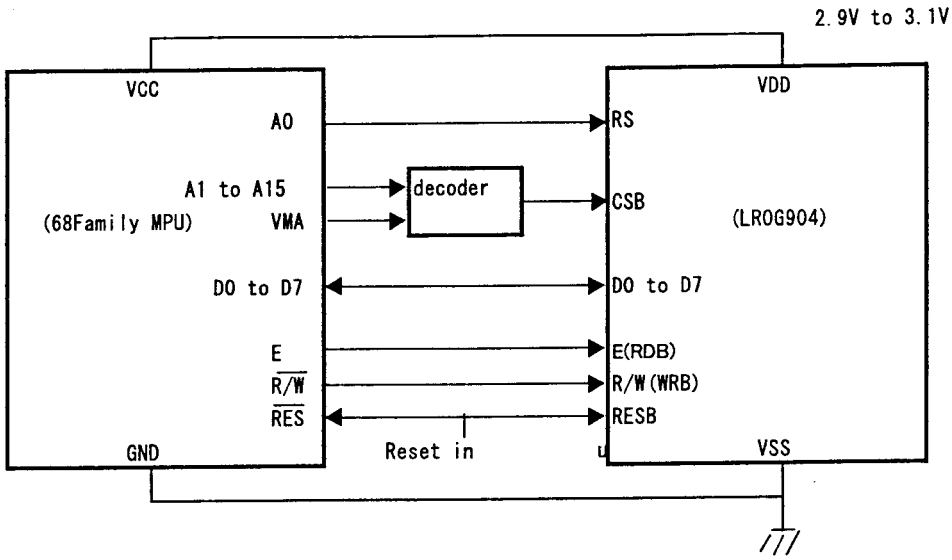
(VDD=1.8～2.4 V, Ta= -15 ～ +60 °C)

Item	Symbol	Measuring condition	MIN	MAX	Unit	Applicable pin
Address hold time	tAH6		50		ns	CSB
Address setup time	tAS6		20		ns	RS
System cycle time	tCYC6		800		ns	E
Enable pulse width	tEW6		500			
Read data output delay	tRDD6	CL=15 pF		400	ns	D0～D7
Read data hold time	tRDH6		10		ns	
Input signal rise and fall	tr, tf			30	ns	All of above pins

Note: All the timings must be specified relative to 20 % and 80 % of VDD voltage.

11. Representative Applications (Connection Example)

Connection to MPU



12. Mechanism Rating

Module appearance drawing Drawing number: SF9-S006

13. Mechanical Characteristics

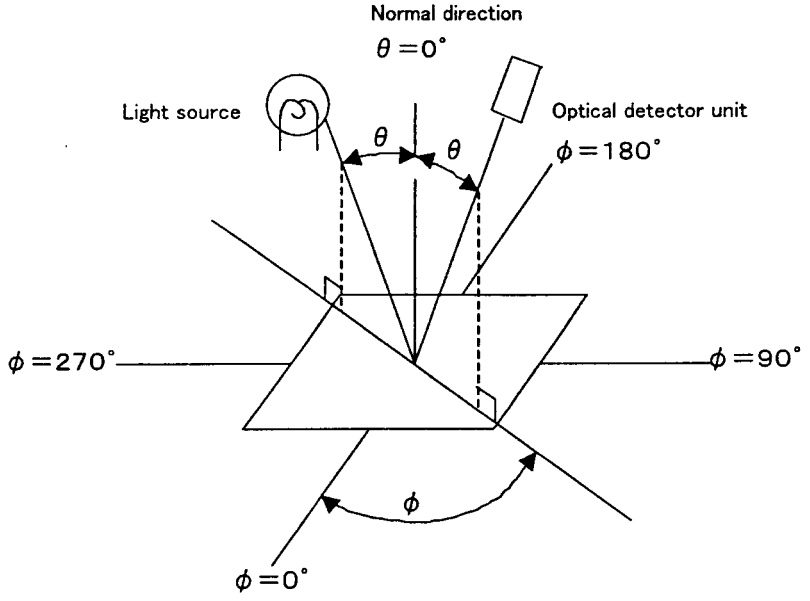
Item	Standard value	Unit
Outside dimension	32.5 (width) x 30.1 (length) x 1.65 (thickness)	mm
Viewing area	28.4 (width) x 22.9 (height)	mm
Active area	25.58 (width) x 20.46 (height)	mm
Number of dots	128 (width) x 64 (height)	
Dot size	0.18 (width) x 0.3 (height)	mm
Dot pitch	0.2 (width) x 0.32 (height)	mm

14. Electrical/Optical Characteristics

Item	Symbol	MIN.	TYP.	MAX.	Unit	Ta	Measurement angle		Remarks
							Optical detector unit	Light source	
Drive voltage	Vop	-	10.6	-	V	-15℃	θ=0° ϕ=0°	θ=30° ϕ=180°	* 1
		-	8.4	-		25℃			
		-	7.8	-		60℃			
Frame frequency	F	-	64	-	Hz	-	-	-	* 1
Contrast ratio	Co	2.0	3.0	-	-	25℃	θ=0° ϕ=0°	θ=30° ϕ=180°	* 1, * 2
Response time	τr	-	170	270	msec	25℃	θ=0° ϕ=0°	θ=30° ϕ=180°	* 1, * 2
	τd	-	320	510					
Viewing angle	θ2-θ1	-	80	-	deg.	25℃	ϕ=0°		* 3
	θ1	-	-40	-20					* 4
	θ2	25	40	-					

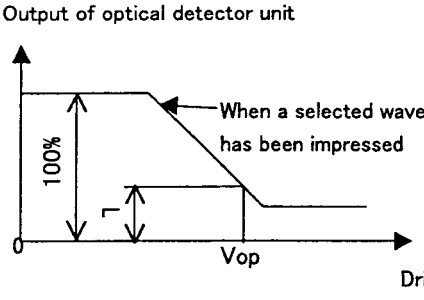
* 1. Drive waveform shall be 1/64 Duty, 1/7 Bias.
* 2. Drive voltage Vop = TYP8.4 V. Frame frequency shall be a typical value of the above-mentioned table.
* 3. Drive voltage Vop = TYP8.4 V. Frame frequency shall be a typical value of the above-mentioned table. Range Co $\geqq$ 1.1
* 4. Drive voltage Vop = TYP8.4 V. Frame frequency shall be a typical value of the above-mentioned table. Range Co = 1.1

(i) Measurement system of electro-optical characteristics



The positions of optical detector unit and light source shall be based on a measurement angle of Item 14.

(ii) Drive voltage Vop



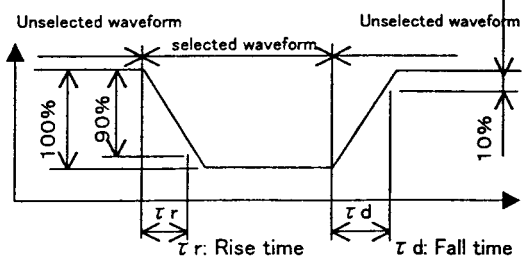
Measurement angle: Measurement angle of Item 14
Drive waveform : 1/64 Duty, 1/7 Bias drive waveform
Frame frequency: Standard value of Item 14

(iii) Contrast ratio

$$(Co) = \frac{\text{Output of optical detector unit when unselected waveform has been impressed}}{\text{Output of optical detector unit when selected waveform has been impressed}}$$

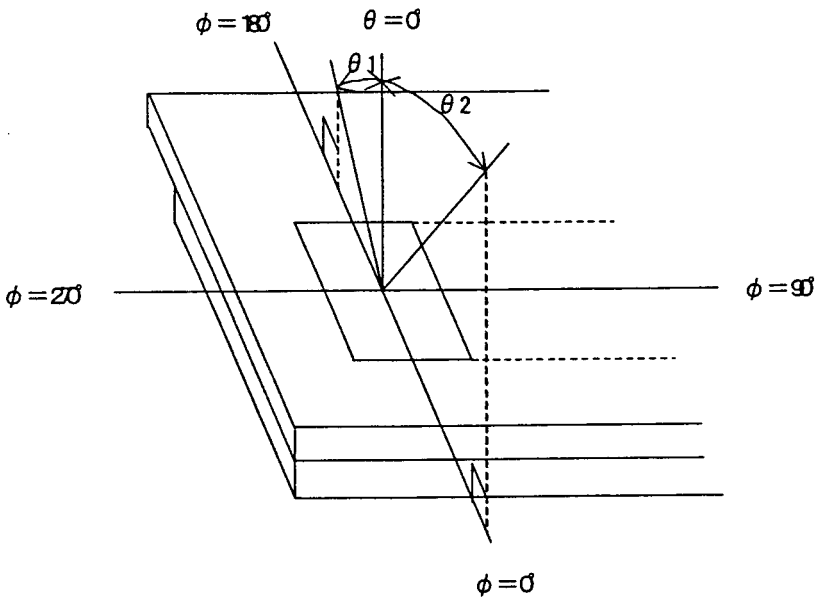
Measurement angle : Measurement angle of Item 14
Drive waveform : 1/64 Duty, 1/7 Bias drive waveform
Frame frequency: Typical value of Item 14

(iv) Response time



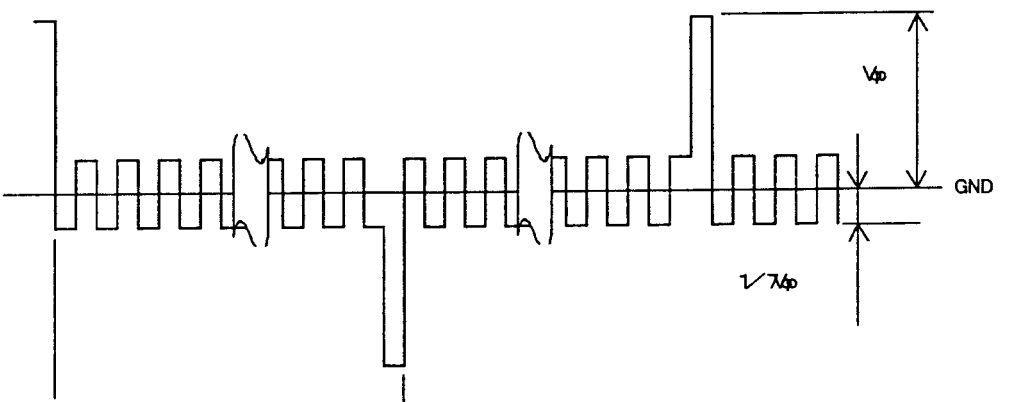
Measurement angle: Measurement angle of Item 14
Drive waveform : 1/64 Duty, 1/7 Bias drive waveform
Frame frequency: Typical value of Item 14

(v) Viewing angle

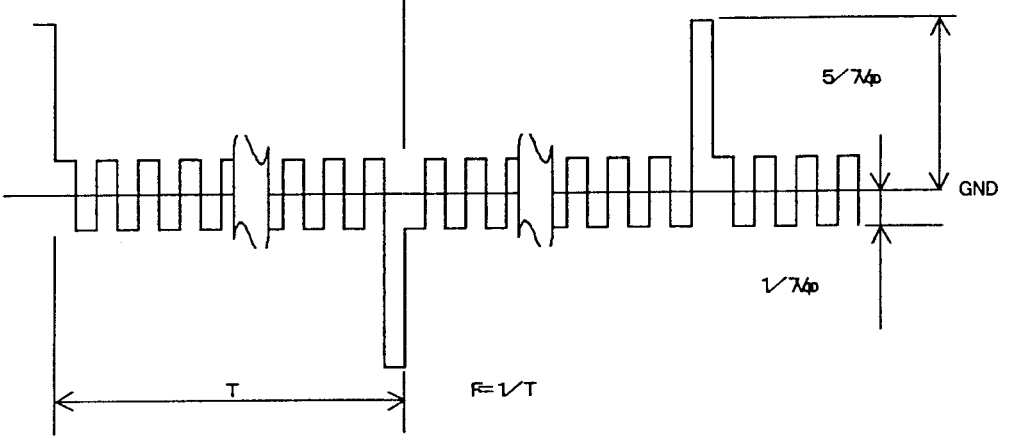


(vi) Drive waveform

Selected waveform



Unselected waveform



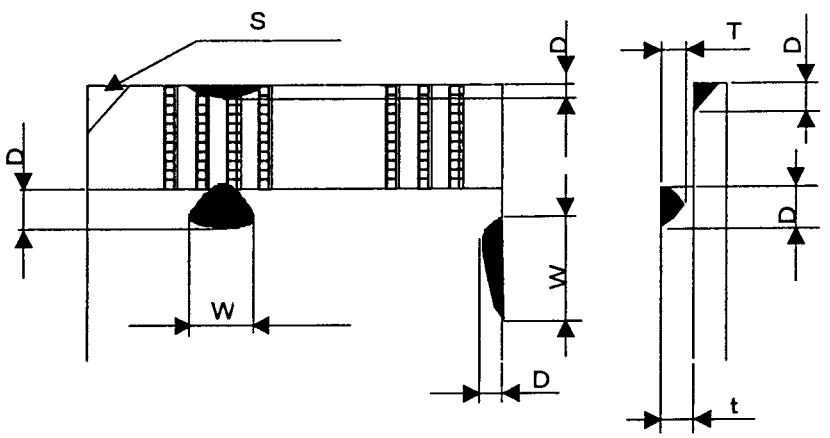
15. Appearance Quality Specifications

15-1. Glossary

(1)	Black point (I) Black line (I)	It looks like a dark dot (black) or line upon lighting and the size is not changed even if the liquid crystal drive voltage varies.
(2)	Black point (II)	It looks like a dark dot upon lighting and the size is changed if the liquid crystal drive voltage varies.
(3)	White point (I) White line (I)	It looks like a light dot or line upon lighting and the size is not changed even if the liquid crystal drive voltage varies.
(4)	White point (II)	It looks like a light dot upon lighting and the size is changed if the liquid crystal drive voltage varies.
(5)	Black line (II)	It looks like a dark line upon lighting and the size is changed if the liquid crystal drive voltage varies.
(6)	White line (II)	It looks like a light line upon lighting and the size is changed if the liquid crystal drive voltage varies.
(7)	Incomplete vertical line	A line in a minor axis direction does not turn on upon lighting
(8)	Incomplete horizontal line	A line in a major axis direction does not turn on upon lighting.

15-2. Appearance standards

Item	Criterion	Classification
Black point (I) White point (I) Foreign material	(1) The below-mentioned are observed in an active and viewing display area. Average diameter: D (mm) <1> Black point (I)/ Foreign material (a) D>0.22 N≧1 (b)0.22≧D>0.1 N≧3 Anything D < 0.1 is not judged. <2> White point (I) (a) D>0.22 N≧1 (b) 0.22≧D>0.1 N≧3 Anything D < 0.1 is not judged.	 Minor defect Minor defect Minor defect Minor defect
Black line (I) White line (I)	(2) The below-mentioned black line (I) / white line (I) is observed in an active and viewing display area. Width: W (mm) Length: L (mm) (a) W>0.05 L≧0.35 N≧1 (b)0.05≧W>0.03 L≧2.0 N≧1	 Minor defect Minor defect

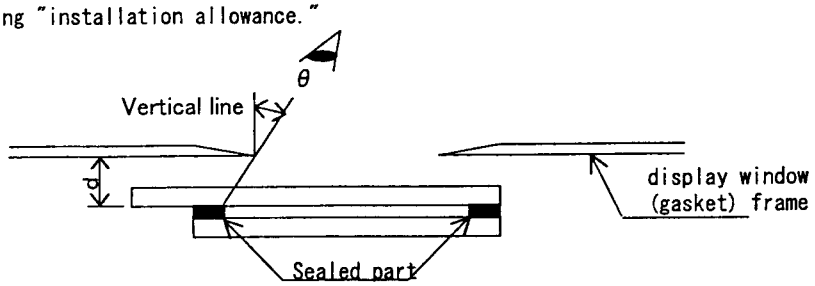
Item	Criterion	Classification
Flaw/dent on polarizing plate	(3) Any flaw/dent in polarizing plate shall comply with the detection of (1) black point (I)/white point (I)/foreign material (2) black line (I) / white line (I).	Minor defect
Glue bubbles and creases on polarizing plate	(4) Visible flowting and peeling of polarizer are observed on a glass surface	Minor defect
Stain on LCD panel	(5) Even if the LCD panel is wiped by soft cloth or something like that, stain is not removed.	Minor defect
Partial discoloration/ color tone on LCD panel.	(6) Upon not lighting, remarkable partial discoloration/uneven color tone is observed in an effective display area.	Minor defect
Breakage/crack in glass	The below-mentioned breakage/crack in glass is observed in a certain area. Width: W (mm) Depth: D (mm) Thickness: T (mm) Area: S (mm) 	

Item	Criterion	Classification
Breakage/crack in glass	(10) Breakage in glass	
	<1> Breakage is observed in a glass edge	
	(a) W>3.0,D>1.0 ,T=t N≧1	Minor defect
	(b) Even within the above-mentioned criterion, breakage is observed in the seal and the seal width is narrowed.	Minor defect
	<2> Breakage in corner	
	(a) S>4.0 N≧1	Minor defect
	(b) Even within the above-mentioned criterion, breakage is observed in the seal and the seal width is narrowed.	Minor defect
	<3> Breakage is observed in an electrode.	
	(a) D>0.8 N≧1	Minor defect
	<4> Breakage is observed in a glass edge	Minor defect
	(11) Crack	
	<1> Crack is observed in a glass edge.	
	W>4.0, D>2.0, T>t N≧1	Minor defect
	<2> Crack is observed in a corner.	
	S>4.0 N≧1	Minor defect
	<3> Crack is observed in an electrode.	
	(a) D>0.8 N≧1	Minor defect

16. Notes on Use

(1) Notes on display window frame

Design the display window frame so that sealed parts cannot be seen from a viewpoint at an angle of θ degrees to the vertical line as shown below, including "installation allowance."



As the distance "d" between the display window frame and liquid crystal display unit becomes small, the sealed parts get invisible.

(2) Note on cabinet assembling

Upon assembling any liquid crystal display device to a cabinet, take care not to impose any considerable stress to it upon working or because of mechanical design. Upon pressing the liquid crystal display device to compress a rubber connector, apply the pressure to sealed parts or a terminal unit uniformly and do not apply any pressure to the inside (display side) of sealed area. Upon assembling, check the direction of end seal of the liquid crystal display device.

(3) UV-resistant

The surface polarizing plate with UV CUT characteristics is used as UV-resistance. Without mounting the surface polarizing plate on the LCD display device, do not leave it alone under the direct sunlight or fluorescent light for a long time.

(4) Distortion of impressed waveform

Minimize any DC voltage due to distortion of impressed waveform.

(5) Cleaning of liquid crystal display device

Upon cleaning the liquid crystal display device, wipe it with soft cloth. Do not use any organic solvent. (Very small amount of petroleum benzine is acceptable.)

(6) Static electricity countermeasure

A polarizing plate, polarizing plate protection film, reflecting plate, etc. are used in LCD and it is easy to be charged with the static electricity. Upon handling, pay attention to the installation of ion blow, grounding, working environment, etc. and prevent the static electrical charge.

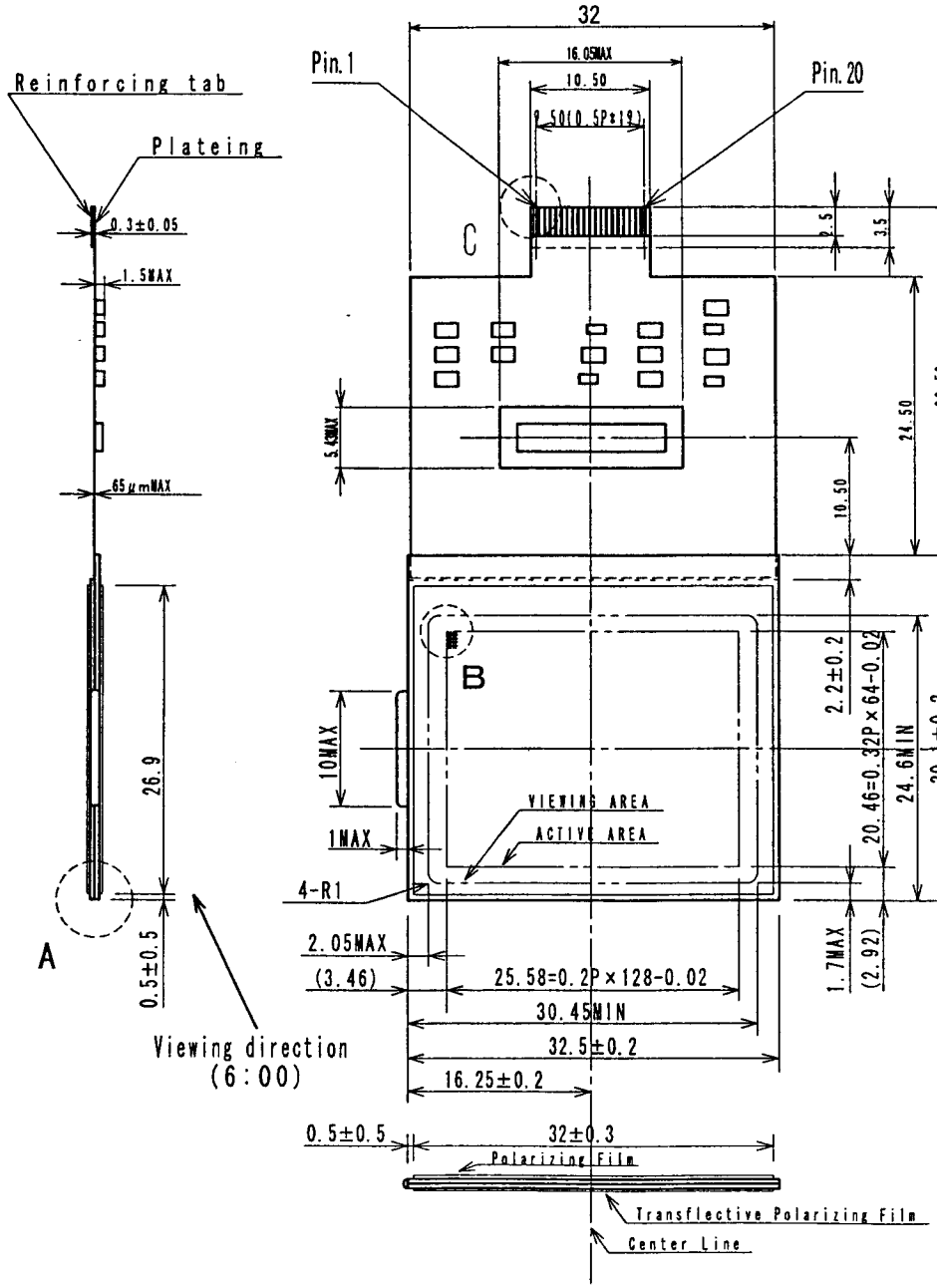
Do not touch a terminal unit directly. Upon using, take any static electricity countermeasure for facility, e.g., contacting the terminal unit by any conductive material.

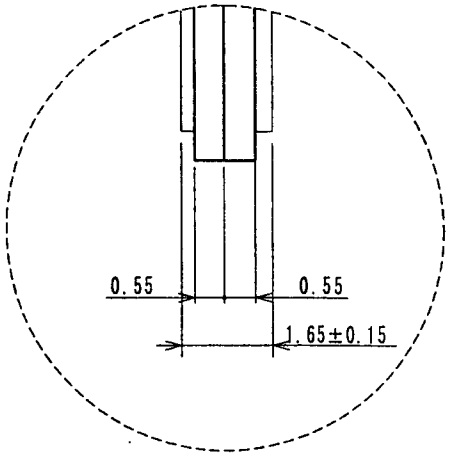
(7) Others

<1> Inform any change in material and process beforehand, which affects the appearance and performance.

<2> If there is any problem in the Specifications, both parties shall discuss and take necessary actions.

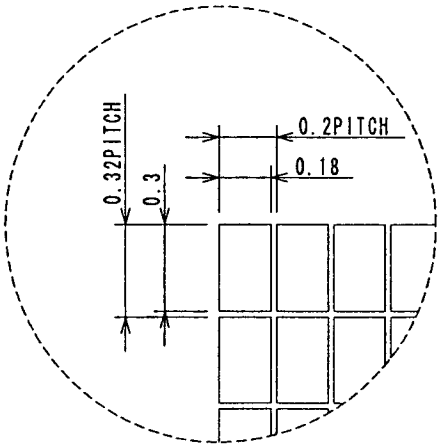
<3> No stain shall be observed completely from on an electrode unit which cannot be wiped with nonwoven fabric and alcohol.



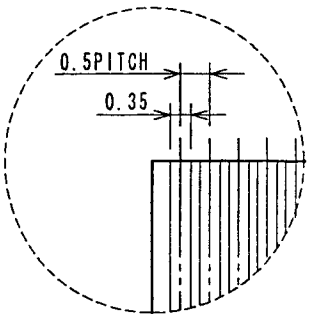


DETAIL:A(S=10/1)

Pin No.	Symbol
1	DUMMY
2	Vss, TEST
3	RESB
4	CSB
5	RS
6	M/S, M86, P/S, SDA, SCL, VDD
7	R/W(WRB)
8	E(RDB)
9	D0
10	D1
11	D2
12	D3
13	D4
14	D5
15	D6
16	D7
17	Vss, CK, CKS, EXA, PMODE
18	VDD, VEE
19	Vss
20	DUMMY



DETAIL:B(S=50/1)



DETAIL:C(S=10/1)

Note.1 1/64Duty, 1/7Bias, FSTN, Transflective, Positive

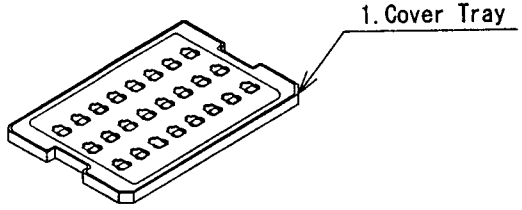
					SCALE	UNIT	
					2/1	mm	
THICKNESS	TOLERANCE		MATERIALS	FINISH			
	±0.5						
DATE	10.27.'99						
DESIGN	TRACE	CHECK	CHECK	APPROVE	INTEGRATED CIRCUITS GROUP		
Y.SHINTANI					MODULE ASSEMBLY APPLICATION ENG DEPT.		
					SHARP CORPORATION		

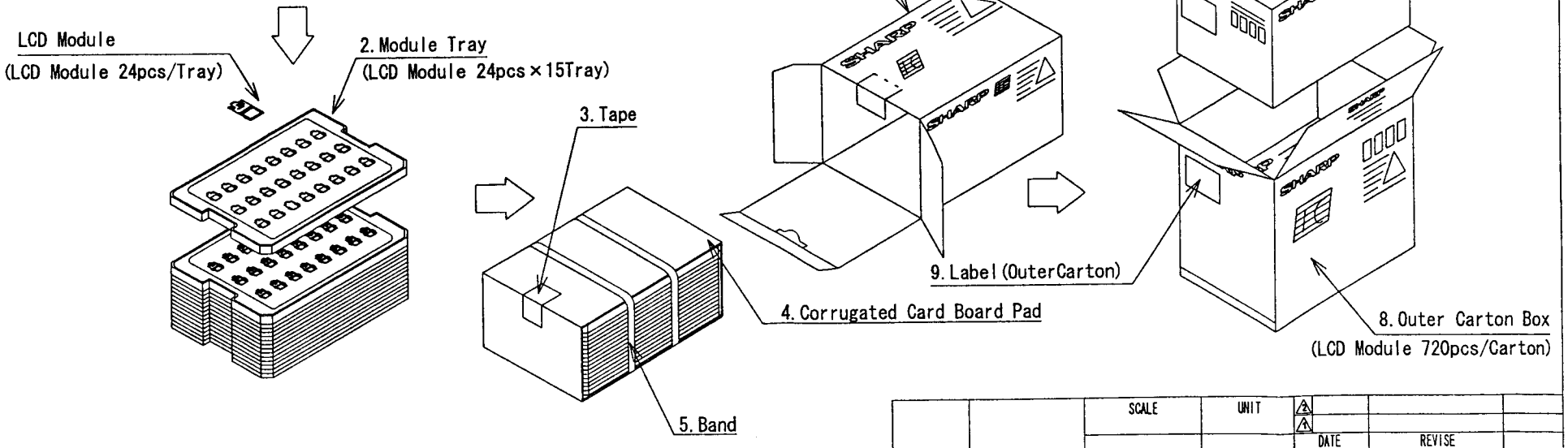
DATE	REVISE
NAME	LROG904 OUTLINE DIMENSION
CODE	
DRAWING No.	SF9-S006

SHARP

17. Packing Specifications

Packing Material (24pcs/Tray, 720pcs/Outer Carton)			
	Type	Spec/Size	Qty
1	Cover Tray	PS (Polystyrene)	2
2	Module Tray	PS (Polystyrene)	30
3	Tape	Paper Tape (Kraft Tape)	2
4	Pad	Corrugated Card Board	2
5	Band	PP (Polypropylene)	4
6	Inner Carton Box	Corrugated Card Board	2
7	Label (Inner Carton)	Label	2
8	Outer Carton Box	Corrugated Card Board	1
9	Label (Outer Carton)	Barcode Label	1





				SCALE		UNIT			
							DATE	REVISE	
THICKNESS		TOLERANCE		MATERIALS		FINISH	NAME	LROG904 PACKAGING DRAWING	
DATE		10. 27. '99					CODE		
DESIGN	TRACE	CHECK	CHECK	APROVE	INTEGRATED CIRCUITS GROUP				
H. TOMOKUNI					MODULE ASSEMBLY APPLICATION ENG. DEPT.		DRAWING No.	SF9−H007	
					SHARP CORPORATION				