DISPLAY DEBUGGING

Connecting a flat panel LCD display for the first time can be a difficult task. Depending on the level of integration the engineer task may range from plugging in a cable to developing a custom ASIC. Typically most flat panel problems revolve around the interconnect cable. The scope of this debugging chart is to assist an engineer in getting the display to operate, correctly.

Recommended Equipment

The following equipment is recommended for debugging displays: a multimeter and a 200 MHz oscilloscope. These are very important, In order to be able to confirm that the correct signal is making it to the display. Trying to debug a display by pulling on wires or squeezing cables is only guessing.

Damaging the Display

Improper input timing will not damage a display when applied for short periods of time. The display may be damaged if power is misapplied. Double check all supply and contrast voltages at the LCD connector cable before connecting the display.

CONTROL SIGNAL INTERCONNECT CHART

When connecting a LCD flat panel to a video controller, it is not always obvious how the two are connected. There are three primary signals required to drive the display, horizontal sync, vertical sync, and dot clock. Depending on the display type, these signals may be labeled differently, but they have the exact same function.

Table 1. Control Signal Interconnect Chart

DISPLAY SIGNAL NAME			CONNECTS TO	COMMON VIDEO SIGNAL NAME	SIGNAL DESCRPTION
PASSIVE COLOR	TFT DISPLAY	MONOCHROME			
XCK	CK	CP2	→	Dot Clock	Pixel Clock
LP	Hsync	CP1	→	Horizontal Sync, LP	Start of Horizontal Line
YD	Vsync	S	→	Vertical Sync, FLM	First Line Marker, Start of Frame
DISP		DISP	→	Display Enable	Controls Display Operation
	ENAB		→	Data Enable	Horizontal Centering Control

Basic Problems

The following is a simple chart for debugging a flat panel display. The symptoms are listed on the left side of the column and the possible causes are on the right, with the most basic problems listed first to display specific fine tuning at the end.

Table 2. Basic Debugging Chart

SYMPTOM	POSSIBLE PROBLEM
Display is completely black	Backlight is not operating. 1. Backlight is not hooked up, verify that the connector is plugged in completely. 2. Check that backlight inverter can supply the correct voltages and current for the backlight. 3. Check that the correct voltages are being applied to the inverter. Most inverters have an on/off control signal, be sure it is set to on. 4. Backlight tube has been damaged.
Backlight is on but no display	Sync signals and Display supply voltage are not being driven correctly. Even if the signals are out of range an LCD module will display some sort of information. Specifically check Hsync, Vsync, Dot Clock, and the input voltages. 1. Be sure data input connector is seated correctly. 2. Verify that the data cable is wired correctly. Please refer to the interconnect table for signal names and connections. 3. Verify the input signals are at the correct active level and are within the display's specifications. Always check these signals at the input connector. 4. With display hooked up verify that contrast and supply voltages are still with specification. 5. Verify contrast voltage on passive displays are within specification 6. Check power sequencing. Improper power sequencing can result in latch up. Do not assert sync signals without V_{CC} applied in the correct sequence.
Information visible but badly scrambled on display	Input signals to the display are not correct. The LCD module will try to operate if the input signals are close to correct. 1. Check Hsync, Vsync, and Clock to be sure they are within specification limits. 2. Be sure V_{CC} and sync signals do not have excessive noise. 3. Verify at the input connector that the each pin has the correct signal.
Information is correct, but data jitters or blurs	Clock to Data setup and hold time is being violated or excessive noise on data. Cable length is usually the culprit here. There is no easy fix for trying to drive a high speed TTL signal several feet. 1. Reduce cable length to as short as possible. 2. Reduce loading on dot clock signal. 3. Add termination to clock line. 4. Use high quality cable for interconnect. 5. Buffer output signals.
Display jumps vertically	Noise on Vsync is causing false triggers to the LCD state machine. 1. Reduce cable lengths. 2. Add in line resistance to Vsync line. 3. 1 pF cap on Vsync to filter noise.
Image tears or jumps horizontally	Noise on Hsysc is causing false triggers to the LCD state machine. 1. Reduce cable lengths. 2. Add inline resistance to Hsync line. 3. 1pF cap on Hsync to filter noise.

TECHNOLOGY SPECIFIC ISSUES

Passive and active matrix displays each have different issues regarding debugging. The next section is broken into two groups regarding each.

Active Matrix (TFT)

Active matrix displays operate at the highest dot clock frequencies of all the technologies. TFTs usually operate at one or two pixels per clock. Because of their exceptional color range, TFT's also have the most data bits. Consequently, TFTs have a lot of digital lines that operate at high data rates. Most designers would gasp at the thought of trying to operating their 25 MHz RISC processor on anything less than a four layer board, yet try to operate a 40 MHz SVGA display over a two foot ribbon cable. TFT's also have to latch a 6 or 8 bit binary number for each color. At 8 bits per color a TFT will have 24 data lines. It is very easy to miswire the data lines.

Passive Displays

Unlike active displays, some passive displays operate at a much lower dot clock rate. The video controller must output several pixels per clock (up to eight in the case of monochrome). Passive displays are much more tolerant of setup and hold issues than active displays. Passive displays however, require an external contrast control for the display. Passive displays are also much more sensitive to changes in temperature and vertical frame rates.

Table 3. Active Matrix Debugging Chart

SYMPTOM	POSSIBLE PROBLEM
Colors are not correct	The data lines between the controller and the display are not connected correctly. 1. Wiring error. Verify connections between display and controller. 2. Controller is configured wrong. Many video controllers have multiple function pins. Verify the video controller is programmed with the correct number of bits per color.
Display is jittery and image breaks up	Data is being latched on the wrong edge of the clock. 1. XGA displays use the rising edge of the dot clock to latch data. This is different from most other display technology. Verify that the data is valid during the rising edge, invert clock if necessary.
Display is shifted horizontally	DE, data enable not operating correctly. TFT displays use the data enable signal to center the data on the display. 1. Verify that DE is within spec at the output connector. 2. Verify that the video controller is generating DE. Some controllers use a programmable pin for this signal.
Pixels appear to be doubled on the display	Some SHARP displays operate at two pixels per clock. Verify that the controller is outputting two pixels per clock.

Table 4. Passive Matrix Debugging Chart

SYMPTOM	POSSIBLE PROBLEM
Display appears 'washed out', poor contrast	Contrast voltage is not set correctly. There is no exact voltage setting for all passive displays. Most designs allow for external control of the contrast voltage. 1. Verify contrast is set correctly at optimum level. 2. Verify vertical sync timing is correct.
Cross talk or shadowing is displayed on screen	If the vertical sync rate is too high, banding will become more pronounced. Reduce vertical frame rate by either reducing dot clock or extending Hsync active times.
Display loses uniformity after operating for extended periods	Contrast on passive displays change over temperature. Check clearances between hot components and the display.
Background is too dark on monochrome display	Contrast voltage is not set correctly.

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